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Resonant current estimation and phase-locked loop feedback design for piezoelectric transformer-based power supplies

Zijiang Yang, Jack Forrester, Jonathan N. Davidson, Martin P. Foster and David A. Stone

***Abstract*—A control system to achieve zero-voltage switching (ZVS) for an inductorless half-bridge piezoelectric transformer-based resonant power supply is presented. Both the phase and frequency of the resonant current are locked to the switching waveform using an analogue phase-locked loop (PLL) to ensure ZVS operation. We present two resonant current estimation circuits which generate the reference signals for the PLL. We also present three PLL feedback designs to produce the in-phase gate drive signals with adequate deadtime. The operating principle of the control system and its ability to achieve ZVS operation is discussed. Experimental results of the PLL circuit verify the successful operation of the proposed system. The six permutations of current estimation and feedback are contrasted and conclusions for application-specific usage are made.[1]**

***Index Terms*—piezoelectric transformer, resonant power supply, phase-locked loop, zero-voltage switching**

I. Introduction

PIEZOELECTRIC transformer-based switched-mode power supplies (SMPS) have been commercialized for many applications [1]–[4]. Compared to magnetic transformers, they exhibit low electromagnetic interference, high power density, high efficiency and reduced weight [5]–[8]. Additionally, the manufacturing process of piezoelectric transformers (PTs) is simpler than for electromagnetic transformers because core assembly and windings are not required. However, PTs experience fundamental limits on energy transfer due to strain, surface charge density, stress, electric field strength and mechanical losses [9][10]. As reported in the literature, 97% efficiency has been achieved for a radial vibration mode PT [11]. The power rating for PTs ranges from 5W/cm^3 (longitudinal vibration mode double polarization PT) to 40W/cm^3 (radial vibration mode thickness polarization PT) with a typical power of 40W [11]. PTs show a resonant peak around their natural frequency since they are usually constructed from high-quality materials such as lead zirconate titanate (PZT). For high efficiency and high-power operations, PTs normally operate in a narrow frequency band close to their primary resonant frequency, with a matched load at the output of the transformer. The optimum operating frequency of a PT is dependent on parameters including load, temperature, geometric design, PT vibration mode (e.g. radial, thickness-shear) and material selection [5][12][13].

Several circuit topologies have been investigated to drive PTs, including push-pull [5], class-E [13] and half-bridge [14]. Although the inductorless half-bridge configuration shows the best performance in terms of size and cost, as it eliminates the need for any magnetic components at the expense of increased deadtime and difficulty of control [15][16], the operating frequency is reduced to a narrow band slightly above resonance, where the PT exhibits inductive behaviour.

The control strategies for PT-based converters reported in the literature include pulse-width modulation (PWM) [17], pulse-frequency modulation (PFM) [18], pulse-density modulation [19] and phase-locked loop (PLL) [20]. Specifically, [17] and [20] realize both soft-switching and output voltage regulation, while [18] and [19] only achieve output voltage regulation. In [21], a combination of PWM and PFM is used for line and load regulation of an AC/DC converter. The circuit in [21] employed PWM at a fixed switching frequency for low output voltages and employed PFM at a fixed duty ratio for high output voltage. An overall efficiency of 80% was achieved with a 17V output at 12Ω load over an input voltage range of 90-270V. For PT-based inductorless configurations, an input matching network has been introduced in [19][22] while a self-oscillating control system is implemented in [2] to achieve ZVS.

In [19], pulse-density modulation is employed to regulate the

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output voltage, with an input matching network implemented to reduce switching harmonics, achieving a total efficiency of 80%. A multi-loop control strategy is used to modify the number of on/off cycles, switching frequency, burst-mode period and deadtime which can be dynamically adjusted.

In [20], a phase-locked loop with PWM control is implemented for line regulation. The reference input of the control circuit is generated by comparing the demodulation signal of the secondary voltage and the injected low-frequency reference signal. A 40W DC/DC converter using this control strategy shows a wide soft-switching region independent of load variations, achieving 75% efficiency when supplying 20V at loads ranging from 50Ω to 500Ω. However, each of these control methods reported in the literature experiences one or more of the following drawbacks:-

1) Resonant frequency drift of the PT is uncompensated. The resonant frequency varies with load and temperature [23][24]. As the efficiency of a PT is maximised when it operates close to its resonant frequency, any uncompensated change in resonant frequency can decrease efficiency. Therefore, a highly sensitive adjustable control strategy is required to maintain high-efficiency operation, such as phase-locked loop control [25], adaptive phase control [20] or self-oscillating control [26].
2) The feedback signal is taken from the secondary side of the PT. This is likely to be the only choice for the feedback controller since the power stage is directly coupled to the primary section of the PT. Unless suitable steps are taken, feedback to the power stage bypasses the isolation barrier from the PT and increases the risk of electromagnetic interference (EMI) [27]. Mitigating steps increase the circuit size, increase cost and diminish the benefits of using a PT [1][28]. Hence, approaches which take feedback from the primary side have emerged. Currents and voltages from the Mason equivalent circuit (see Fig. 1) can be estimated/measured, and the converter is switched when the estimated reference signal passes through its zero-crossing or peak [26][29].
3) High efficiency and ZVS are hard to achieve for the inductorless topology. This is because less resonant current is provided during the deadtime[30]. In [19] and [22], an input matching network is introduced for ZVS optimization. However, total efficiency is decreased since part of the energy is consumed by the matching network. Moreover, the PT's driving waveform generated by the matching network is not ideal hence other higher order harmonics are introduced and cannot be ignored in practice. Other solutions such as self-oscillating control have been proposed for the inductorless configuration [2]. With phase compensation introduced in the control loop, the phase angle of total feedback loop is adjusted to an multiple integer of 2π.

To address these problems, a resonant current estimation circuit together with a self-oscillating phase-shift compensation approach were introduced in [26][31]. The resonant current is estimated by an RC network before the PT input section. Current peaks [31] and zero-crossing points [26] of the resonant current are sensed and used for switch timing. The principle of phase compensation is to track the resonant frequency change in a PT with cycle-by-cycle adjustments. An integer multiple of 2π is required for the entire control loop according to Barkhausen criterion, to ensure resonant current and PT input voltage are in-phase. However, when the resonant frequency changes, multi-period lock-in delays can be introduced, which is not desirable for fast tracking. In addition, this approach requires a self-induced oscillation to excite the PT vibration near the resonant frequency during system initialisation. Since the controller must operate as an oscillator and, during start-up, operates with a frequency lower than the PT's resonant frequency for [26], the following problems occur:-

1) The feedback controller becomes unstable due to 180° phase change in the control characteristics [26].
2) The efficiency of the PT is reduced because the converter is operating below the resonant frequency.

Soft switching is not preserved during lock-in delay as the driver has not reached steady state.

In this paper, we present a comparative analysis of six variants of a phase-locked loop (PLL) controller which overcome these problems. Two resonant current estimators and three gate signal generators are proposed and evaluated to mitigate issues of resonant frequency drift, eliminate coupling across the isolation barrier and enable faster circuit initialisation. The designs lock on to the resonant frequency, ensuring $\pi/2$ radians deadtime (demonstrated as necessary in [30]) and therefore achieving zero-voltage switching (ZVS). The controller's ability to lock on to phase and frequency, irrespective of operating conditions and temperature, makes PLL control highly desirable in this application.

The contribution of the proposed work includes: (i) achieving ZVS in an inductorless PT-based SMPS using a PLL, (ii) proposal of two current estimators and their implementation within a PLL, and (iii) proposal of three steering logic and gate signal generators implemented specifically for a 4046 PLL controller.

We draw on the previous work where we developed a design criterion to ensure a PT in an inductorless topology can be operated at the resonant frequency with ZVS for all loads if input-to-output capacitance ratio satisfies $C_{\text{in}}/NC_{\text{out}} \leq 2/\pi$ with $\pi/2$ deadtime [30]. The present paper is organised as follows: the basic operation of PT-based inductorless converters is given in section II, approaches to produce a feedback signal for the controller using current estimators is proposed and explained in section III-A. A mixed analogue-digital implementation of the PLL controller is proposed with different configurations, and given in section III-B. Experimental results, including a comparative analysis, from a practical implementation are shown in section IV to demonstrate the viability of the proposed approach and discuss the choice of topology for different applications.

II. Operation of PT-Based Inductorless Resonant Converter

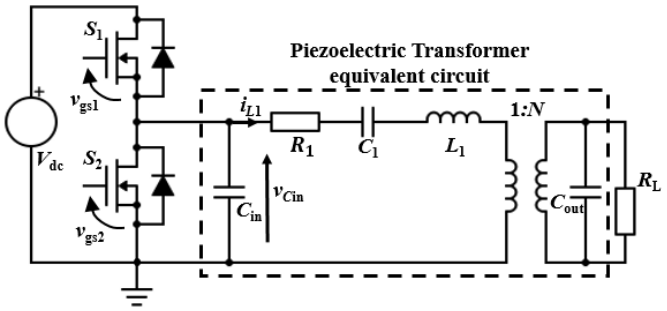

Fig. 1. The inductorless H-bridge PT-based converter with Mason equivalent circuit.

PTs generally have high Q-factor band-pass filter characteristics when they operates close to their primary resonant frequency. There are typically several other modes, but, for a well-designed PT operated close to its primary vibration mode, these can be neglected. Their mechanical resonance and piezoelectric effect can be modelled by the simplified Mason-equivalent circuit as shown in Fig.1 [23][32].

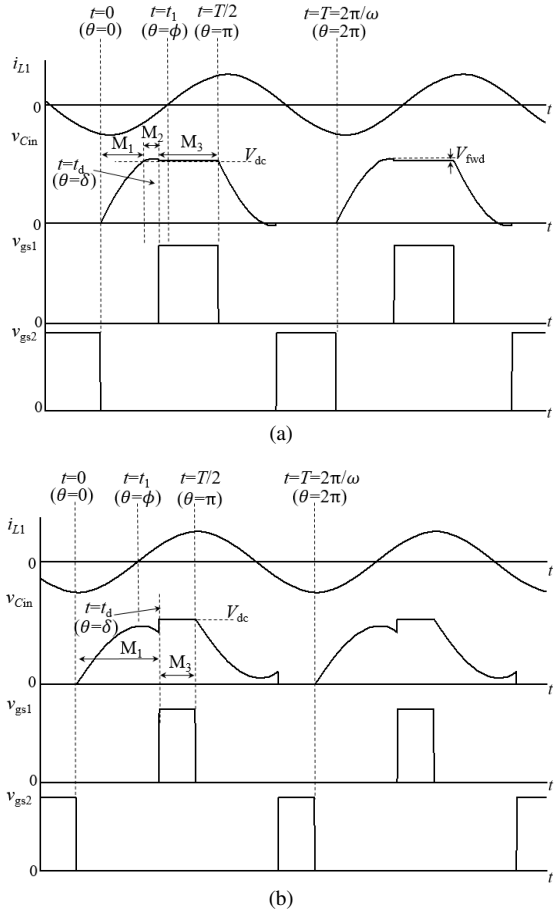

Fig. 2. The switching waveforms of the inductorless H-bridge PT-based converter at (a) ZVS achieved and (b) ZVS not achieved.

C_{in} and C_{out} represent the input and output terminal electrode capacitances, respectively. The acoustic mechanical resonant behaviour is captured by L_1, C_1 and N. R_1 models the effect of mechanical damping and hence power loss in the PT. The half-bridge MOSFETs S_1 and S_2 operate in antiphase. An adequate deadtime is required to provide sufficient input capacitor charging time. Insufficient deadtime results in the input capacitance voltage v_{Cin} failing to reach the DC input voltage V_{dc} before S_1 is turned on thereby generating switching losses.

The typical operation for inductorless PT-based resonant converters exhibits one of following three modes during a half-cycle period.

M1: S_1 and S_2 are off. PT input capacitance voltage v_{Cin} is charged (or discharged) towards the DC input voltage V_{dc} (or 0) by inductor current i_{L1}. This is the deadtime period.

M2: v_{Cin} has exceeded V_{dc} (or fallen below 0) and the body diode of S_1 (or S_2) is conducting, causing v_{Cin} to be V_{fwd} above V_{dc} (or V_{fwd} below 0), where V_{fwd} is the forward voltage drop of the MOSFET body diode.

M3: S_1 (or S_2) is on and v_{Cin} is maintained at V_{dc} (or 0).

The switching waveforms of a PT-based converter are shown in Fig. 2 under two different scenarios: ZVS achieved and ZVS not achieved. The high quality of the resonant tank allows us to assume i_{L1} is sinusoidal. t_d (or δ radians) and t_1 (or ϕ radians) refer to the deadtime and phase delay between PT input capacitance voltage and resonant current, respectively. v_{gs1} and v_{gs2} correspond to half-bridge MOSFET gate drive signals.

In Fig. 2(a), ZVS is achieved following the mode sequence $M_1 \rightarrow M_2 \rightarrow M_3$. During deadtime $0 < t \leq t_d$, the PT input voltage v_{Cin} exceeds V_{dc}, inducing the conduction of the body diode of S_1 until S_1 is turned on at $t=t_d$. Since the MOSFETs are current-bidirectional switches, reverse resonant current flows through S_1 during $t_d \leq t < t_1$. In contrast, the non-ZVS condition is shown in Fig. 2(b) with corresponding switching waveforms. Here, v_{Cin} does not reach V_{dc} during the deadtime and power dissipation occurs due to the near-instantaneous discharge of v_{Cin} as S_1 turns on.

As discussed in [30], a low input-to-output capacitance ratio indicates either less charge required by the input capacitance or more charge available from the resonant current. It results in a reduced deadtime requirement, and therefore makes it easier for v_{Cin} to reach the DC rail (or 0). In terms of load condition, the matched load is the load that gives the lowest resonant current because it is the highest efficiency point [9]. It therefore takes longer to charge the input capacitor during the deadtime period [30]. If ZVS can be achieved at a matched load, ZVS is achievable for all load conditions. The matched load is given as

$$R_L = \frac{1}{\omega_0 C_{\text{out}}} \tag{1}$$

Where ω_0 is the operating frequency [9].

To guarantee ZVS for a PT-based inductorless topology, the design criterion developed in [30] is used in this work. The input-to-output capacitance ratio is set to be $C_{\text{in}}/NC_{\text{out}} = 2/\pi$ with $\pi/2$ deadtime at matched load condition. The input capacitance voltage v_{Cin} is hence maximized at the end of the deadtime interval. When the ZVS criterion is satisfied, the resonant current must be in phase with the MOSFET gate drive signal thereby ensuring that deadtime starts at the negative peak of the resonant current since it is here that the fastest charging of PT input capacitor occurs.

III. Operation of The Proposed ZVS PLL Control System

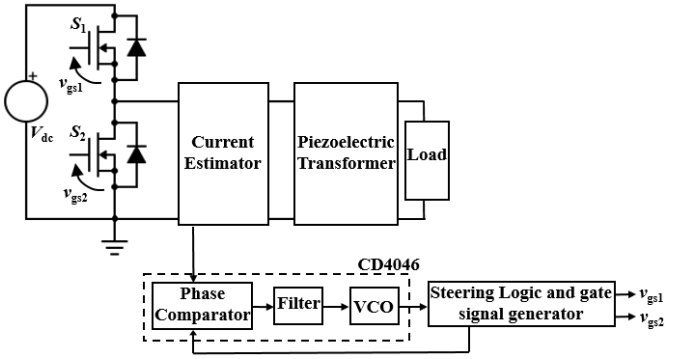

Fig. 3. Block diagram of the ZVS PLL control system.

The proposed ZVS control system consists of resonant current estimation circuit and PLL controller, as shown in Fig. 3. Since the ideal operating frequency of the PT is temperature and load dependent, as well as being subject to manufacturing tolerances. To account for these variations a suitable limits to the operating frequency range, typically ±5% of PT's resonant frequency, must be applied using the PLL.

The PLL controller is implemented by a CD4046 to lock on to the phase and frequency of the resonant current and provide the in-phase switching signals via steering logic to achieve ZVS. A resonant current estimator is employed to reconstruct the Mason-equivalent resonant current as a feedback signal applied to the PLL controller.

The CD4046 consists of the phase comparator, a low-pass filter (LPF) and a voltage-controlled oscillator (VCO). Previous literature on PT-based controller design introduces self-induced oscillation to initialise the PT-based converter, which results in additional circuity and time required for self-excitation of the resonant current [26][33]. This can be eliminated if the VCO range covers only the possible operating frequencies. At the system start-up, when no input signal has been applied to the PLL, the error voltage at the output of the phase comparator is zero. The VCO therefore initially operates at its minimum frequency, which is set close to resonant frequency to ensure a fast system initialisation.

We use the type-II phase comparator of CD4046 which integrates the phase error and therefore ensures, once the PLL has locked on, that the phase error is zero. The LPF performs this integration and also reduces phase noise to produce a stable voltage for the VCO. The PLL's output frequency therefore increases from its minimum until the output is locked in phase and frequency to the resonant current, and ZVS will therefore be achieved if the critical design criterion is met [30].

The performance, complexity and versatility of the controller depends on the particular implementations of the steering logic (which produces the gate signals and phase feedback) and the resonant current estimator. In the following subsections, we present a number of options which provide for six implementations. Each is present and analysed individually, and the final complete implementations are compared. Both simulation and experimental results are provided to demonstrate the versatility of the proposed control systems. A matched load is applied in this work since it indicates the most challenging operating ZVS condition [24]. If ZVS is achieved at the matched load, ZVS operation is possible at any load.

A. Resonant Current Estimation

We will present two current estimation techniques. The first is well known in literature [34], but needs careful differential amplification and requires additional resistance. We subsequently propose a new technique, based on similar mathematics, which eliminates the need resistors and does not need a differential amplifier.

1) Current Estimator 1: Voltage differentiator

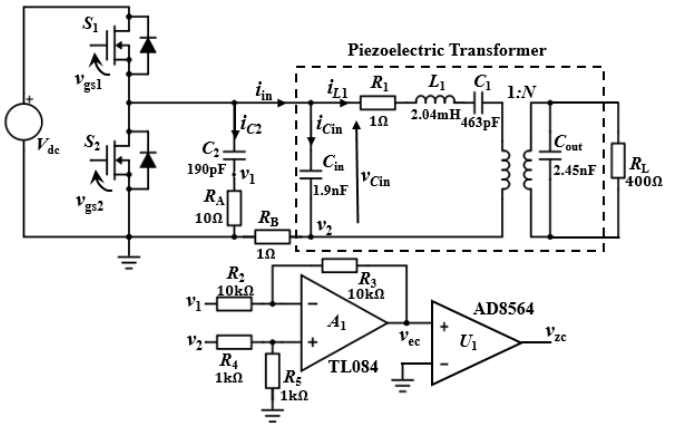

Fig. 4. Current estimator 1 (the voltage differentiator)

Current estimator 1, shown in Fig. 4, differentiates the PT input voltage v_{Cin} to estimate the capacitor current i_{Cin} during deadtime. C_2 and R_A form an approximate differentiator if $R_A C_2 \ll T$, where T is the switching period. The mid-point voltage v_1 provides a derivative signal of the PT input voltage v_{Cin}. During dead-time, the capacitor currents for C_{in} and C_2 can be found (assuming $R_A C_2 \ll T$ and $R_B C_{in} \ll T$) from

$$i_{Cin} = C_{in} \frac{dv_{Cin}}{dt} \quad (2)$$

$$i_{C2} = C_2 \frac{dv_{Cin}}{dt} \quad (3)$$

$$v_1 = i_{C2} R_A \quad (4)$$

Solving (1) to (3) results in

$$v_1 = \frac{R_A C_2}{C_{in}} i_{Cin} \quad (5)$$

which shows that v_1 is a scaled version of the PT input capacitor current i_{Cin}.

The PT input current i_{in} is detected by the sensing resistor R_B. Since

$$i_{in} = i_{Cin} + i_{L1} \quad (6)$$

$$v_2 = (i_{L1} + i_{Cin}) R_B \quad (7)$$

Substituting (4) into (6) and rearranging provides the (7) for the resonant current.

$$i_{L1} = \frac{v_2}{R_B} - \frac{v_1 C_{in}}{R_A C_2} \quad (8)$$

The resonant current, i_{L1}, can be estimated using a differential amplifier. R_2, R_3, R_4 and R_5 set the gain as

$$v_{\mathrm{ec}} = v_2 \frac{R_5/(R_4+R_5)}{R_2/(R_2+R_3)} - v_1 \frac{R_3}{R_2} \tag{9}$$

Comparing (8) and (9), it can be seen that with careful selection of component values, $v_{\mathrm{ec}} \propto i_{L1}$.

It should be noticed that the total effective capacitance at the PT input is increased since C_2 is introduced, ZVS is harder to achieve. Therefore, C_2 should be much smaller than C_{in} in order to minimise its effect on PT performance and the ZVS capability [2][24] (e.g. ten times smaller).

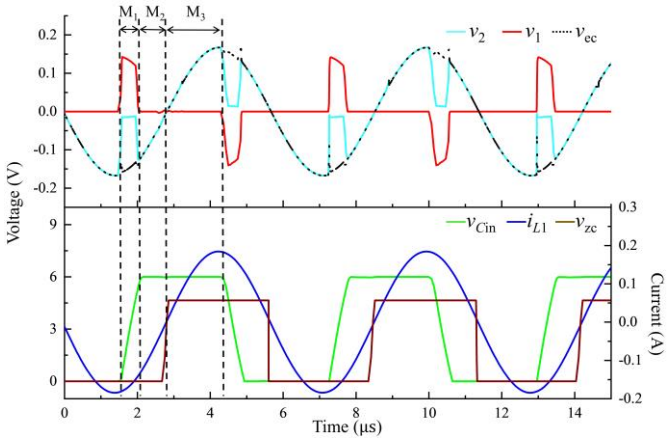

Fig. 5. Operating waveforms of current estimator 1.

The operating waveforms of current estimator 1 under ZVS are shown in Fig. 5. During M_1, the PT input current i_{in} and its scaled representation v_2 remain zero since the PT input capacitor C_{in} is being charged towards V_{dc}. The current through C_{in} and its scaled version v_1 increase accordingly. Once the PT input capacitor has been fully charged, i_{in} is dominated by resonant current i_{L1} which flows in the reverse direction and the body diode of the MOSFET conducts during M_2. During M_3, $v_{C\mathrm{in}}$ is maintained at V_{dc}, therefore its derivative signal v_1 is zero. Voltages v_1 and v_2 are combined to rebuild the estimated resonant current v_{ec} as shown in Fig. 5. A sign-detecting comparator U_1 provides feedback v_{zc} for the controller.

2) Current Estimator 2: Anti-parallel diode sign detector

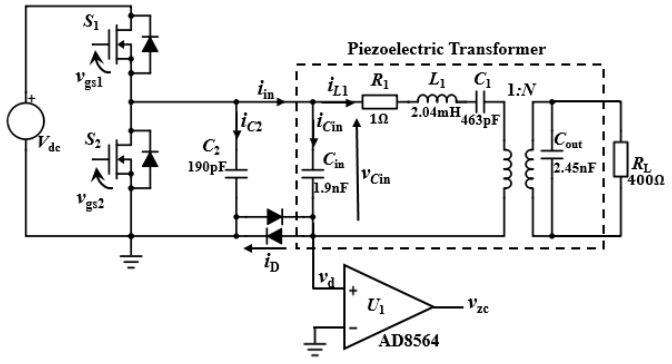

Fig. 6. Current estimator 2.

Current estimator 2, shown in Fig. 6, consists of two anti-parallel diodes coupled to the input section of the PT. These diodes are used to detect the zero-crossing of the resonant current. Each diode current is described by the Shockley equation

$$i_d = I_{\mathrm{s}}\left(\exp\left(\frac{qv_D}{nkT_a}\right) - 1\right) \tag{10}$$

where v_{D} is the voltage across the diode, T_{a} is absolute temperature, k is Boltzmann's constant, n is the emission coefficient, q is the electronic charge and I_{s} is the reverse saturation current. Employing (10) to the anti-parallel diodes configuration results in (neglecting the "-1" term)

$$i_D = 2I_{\mathrm{s}} \sinh\left(\frac{qv_D}{nkT_a}\right) \tag{11}$$

A silicon fast switching diode 1N4148 is employed in this design for easy sign detection of the input current. The reverse-recovery time of 1N4148 is 4ns which is negligible in comparison to the 6μs switching period. There is negligible change in the conducting diode's forward voltage when the current is above 10mA. Since this is much less than the typical current (above 50mA), we can safely assume the forward voltage is constant and merely changes sign with current. Similar to current estimator 1, a capacitor C_2 is connected in parallel to PT input to as shown in Fig. 6 and it is chosen to be much smaller than C_{in} (e.g. ten times smaller) in order to minimise its effect on ZVS capability [2]. Note that no series resistor is required.

The anti-parallel diode current and PT input capacitor current are given as

$$i_{\mathrm{in}} = i_{C\mathrm{in}} + i_{L1} \tag{12}$$

$$i_{C\mathrm{in}} = -\begin{cases} i_{L1} + i_{C2}, & \mathrm{M1} \\ 0, & \mathrm{M2, M3} \end{cases} \tag{13}$$

therefore

$$\frac{\mathrm{d}}{\mathrm{d}t} v_{C\mathrm{in}} = \frac{i_{C2}}{C_2} = \frac{i_{C\mathrm{in}}}{C_{\mathrm{in}}} \tag{14}$$

Solving (12)-(14),

$$i_D = i_{L1} \cdot \begin{cases} 1 + \frac{C_2}{C_{\mathrm{in}}}, & \mathrm{M1} \\ 1, & \mathrm{M2, M3} \end{cases} \tag{15}$$

Therefore i_D and i_{L1} share the same polarity under all modes.

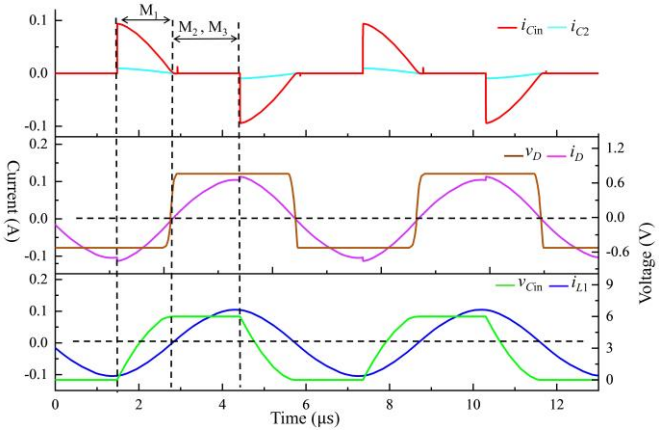

Fig. 7. Operating waveforms of current estimator 2.

Circuit operating waveforms of current estimator 2 are shown in Fig. 7. During M_1, both C_2 and C_{in} are charged towards V_{dc} and the capacitor current i_{C2} is proportional to i_{Cin}. Both i_{C2} and i_{Cin} remain zero once the total PT output capacitance is fully charged. In Fig. 7, i_D is contributed to by i_{C2} and i_{Cin} during M_1 and, for the component values in Fig. 6, it is 1.1 times larger than resonant current i_{L1} as given in (15) (since C_2 is set to be 10 times larger than C_{in}). During M_2 and M_3, i_D is dominated by i_{L1} since C_2 and C_{in} are fully charged. As shown in Fig. 7, i_D and i_{L1} share the same zero-crossing points under all modes. Since the effective signs of i_D can be indicated by anti-parallel diode voltage v_D, v_D represents the sign (i_{L1}) and so can be used by the PLL. A comparator U_1 is used to provide the feedback signal v_{zc} for the controller.

B. *Steering Logic and Gate Signal Generators*

1) *Phase locked PWM*

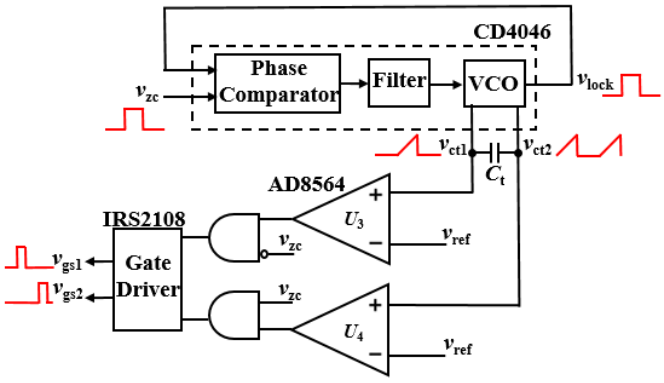

Fig. 8. PLL controller with phase-locked PWM.

The PLL controller with phase-locked PWM (Fig. 8) is implemented by employing the CD4046's timing capacitor voltage (seen as two sawtooth waveforms with 180° phase shift) as a reference signal to produce gate drive signals. The VCO has a 50% duty cycle and operates by charging the external timing capacitor, C_t, via a current source controlled by the VCO input signal. One side of C_t is held at ground while the other side is charged by the current source, producing a ramp (sawtooth) waveform phase locked to the PLL input signal (i_{L1}). Once C_t charges to half of the internal logic voltage, the charged side is pulled to ground, and the other side is discharged trough an internal resistor. A new half cycle begins. The voltage on each side of C_t is shown as v_{ct1} and v_{ct2} in Fig. 8. v_{ct1} and v_{ct2} act as the carrier signals for the phase offset comparator U_3 and U_4 [25], which compare to a carefully valued reference voltage. Subsequently, through the combinational logic, the phase and frequency-locked MOSFET gate drive signals are generated, featuring $\pi/2$ deadtime interval.

2) *RC Time Delay*

Fig. 9 shows an alternative implementation where the controller essentially forms an RC delay circuit by taking the PLL output v_{lock} as a reference. Once the PLL locks onto the resonant current i_{L1}, the PLL output v_{lock} follows the phase and frequency of i_{L1}. In Fig. 9, v_{lock} and its inverted version are shaped through identical RC delay circuits to trigger the gates following the correct delay. The circuit and reference voltage are arranged to provide $\pi/2$ deadtime, ensuring the high-side switch turns on at zero phase and maintains π radians delay between the two switches.

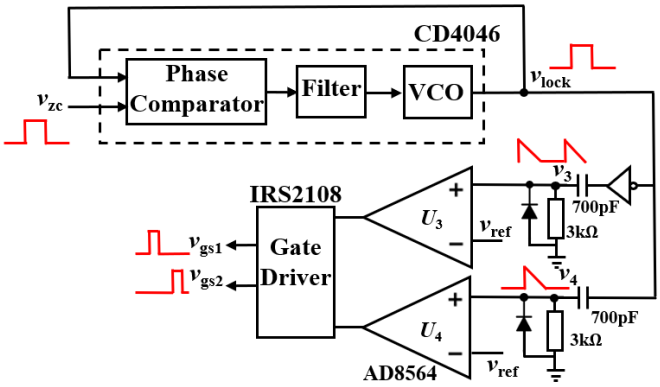

Fig. 9. PLL controller with RC time delay.

3) *Frequency Divider*

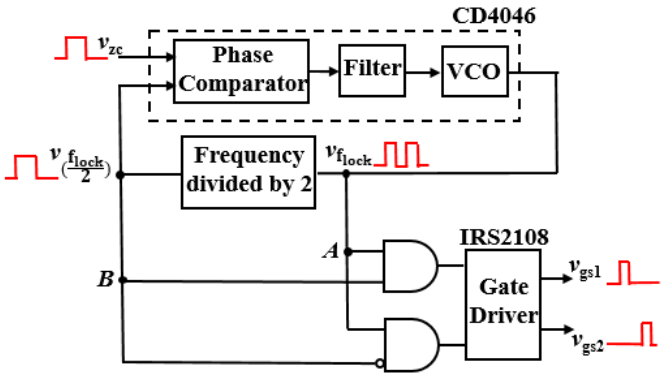

Fig. 10. PLL controller with frequency divider.

Fig. 10 shows an alternative approach where the PLL controller is implemented by employing a frequency divider to the feedback path between the VCO output $v_{f_{lock}}$ and the phase comparator input v_{zc}. A D-type flip flop is used for the frequency divider. The VCO operates at twice the switching frequency, and its halved version is used to drive the half-bridge. With VCO output $v_{f_{lock}}$ (or A) and frequency divider output $v_{(\frac{f_{lock}}{2})}$ (or B), the corresponding in-phase gate drive signals with $\pi/2$ phase shift are generated through combinational logic, according to these Boolean equations:-

$$v_{gs1} = A \cdot B \quad (16)$$

$$v_{gs2} = A \cdot \bar{B} \quad (17)$$

IV. Results and Analysis

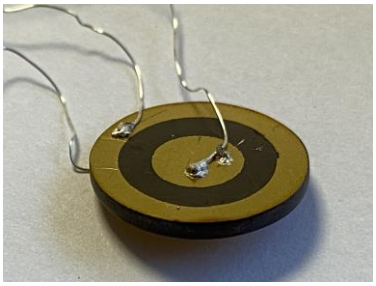

Fig. 11. The ring-dot radial mode piezoelectric transformer under test.

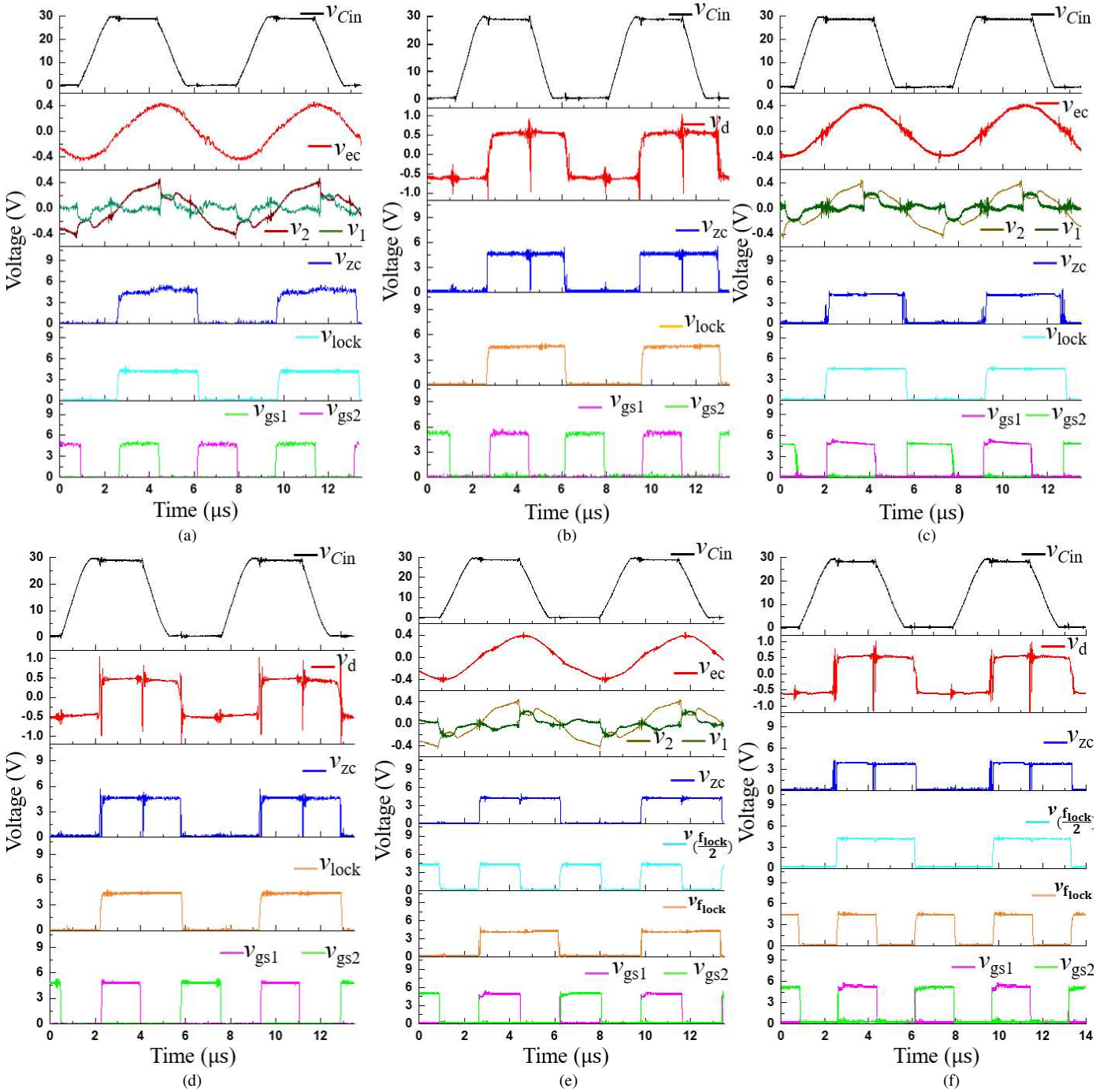

Fig. 12. Experimental results of the proposed control methods. Phase-locked PWM with (a) current estimator 1 and (b) current estimator 2. RC time delay controller with (c) current estimator 1 and (d) current estimator 2. Frequency divider controller with (e) current estimator 1 and (f) current estimator 2.

To show the validation of the proposed control methods, a prototype resonant converter is implemented using a radial mode PT presented in previous work [35][36], as shown in Fig. 11, with the following extracted equivalent circuit component values at a matched load condition:C_{in} =0.43nF, C_{out} =1.14nF, L_1 = 17.2 mH, C_1 =77.8 pF, R_1 =12.5 Ω, N =0.94, Q =1190. The experimental waveforms are shown in Fig. 12.

In these implementations, we use a low supply voltage (30V) to compensate for the low-noise environment of testing laboratory in comparison to typical applications (such as auxiliary supplies in proximity to noisy switching circuits). This does not affect the current sensing and steering logic performance as sensing components are sized to the current (e.g. the current-sense resistor is sized to provide a certain voltage) and the PLL operates at typical logic voltages regardless of load requirements.

For all cases, the PLL internal low-pass filter, which has a corner frequency of 400kHz, is used to compensate the loop and to minimise phase error. For the phase-locked PWM (Fig. 12(a) and (b)) and the RC time delay (Fig. 12(c) and (d)) steering logic implementations, the VCO is restricted to operate between 135kHz and 145kHz by a 410pF timing capacitor, 50kΩ timing resistor and a 200kΩ frequency offset resistor to ensure adequate lock and capture range while still accommodating

component tolerances. For the frequency divider implementation (Fig. 12(e) and (f)), the VCO is set up to cover a lock and capture range of 270-290kHz (i.e. covering twice the resonant frequency) by a 220pF timing capacitor, 90kΩ timing resistor and 500kΩ frequency offset resistor. As shown in Fig. 12, for all cases, the two inputs of the phase comparator of the CD4046 have identical phase and frequency, indicating the PLL-locked condition. The zero-crossing points of the resonant current are clearly shown by the rising and falling edge of v_{zc}. Subsequently, gate signals v_{gs1} and v_{gs2} are generated through the appropriate steering logic and driver circuits.

All results show ZVS achieved (indicated by the v_{Cin} rise completing during the deadtime). As these experiments were performed for the matched load, which is the worst-case condition, they demonstrate the ZVS-capability of the implementations for all loads. This is to be expected as the radial mode PT was designed to meet the critical criterion (see [30]). In each case, v_{zc}, the detected current phase, has clean edges which align to the detected current and the gate signals. Although the noise is not negligible, the results show good agreement with the simulation results (Fig. 5 and Fig. 7), confirming the accuracy of the simulation.

A. *Tracking performance*

1) *Noise immunity*

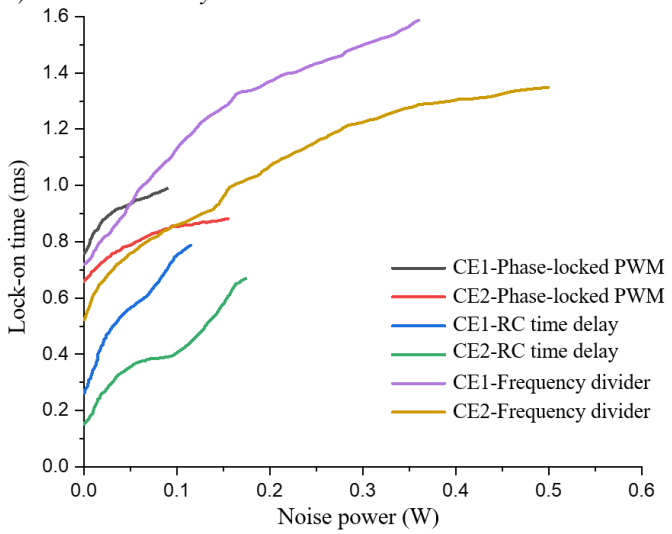

Fig. 13. Lock-on time comparison of the proposed PLL controllers associated with current estimator 1 (CE1) and current estimator 2 (CE2) under noise condition.

To indicate the resonant-frequency tracking performance of all six methods, white noise of varying power is applied to the comparator input of the PLL in simulation and the time taken to lock-on is measured. The simulation test conditions are those in Fig. 4 and the noise power is measured with respect to 1Ω. The results are given in Fig. 13. Where the graphs end prematurely, this is because lock-on was not possible at that level of noise power (i.e. lock-on time was infinite). As can be seen, current estimator 2 (CE2) shows better noise tolerance than current estimator 1 (CE1) regardless of PLL controller type. The frequency divider controller with CE2 gives the best result overall and is able to handle up to 0.50W noise power. In terms of the lock-on time, at a given noise power level, CE2 shows a shorter lock-on time than CE1 for all three steering logic implementations.

The controller noise immunity is significantly improved by the frequency divider approach. This can be explained that as the noise power level increases, VCO will be affected and appears as phase noise on the output of the VCO. In general, phase noise can be generated by PLL itself (e.g. phase detector dominates the noise source within the loop bandwidth while VCO is the dominant noise source outside the loop bandwidth), frequency divider and the resonant circuit [37]. Phase noise from frequency division is negligible when division ratio is small, and it is insignificant when PLL operates at low frequencies. Therefore, the overall PLL noise performance is mainly determined by the resonant circuit [38]. The noise reduction for a given frequency division is $20\log_{10} N$, where N is the division ratio [37]. Hence, a frequency divide-by-two results in an improvement of 6dB (or $20\log_{10} 2$) for phase noise correlated to the carrier frequency (VCO centre frequency), and 3dB (or $10\log_{10} 2$) improvement for the uncorrelated phase noise [38], making a practical and effective way to reduce phase noise of the PLL.

Although CE2 has advantages over CE1 in terms of lock-on time and system noise immunity as indicated in Fig. 13, it experiences larger power consumption compared with CE1 for each PLL controller. To ensure a fair comparison, the forward voltage of the anti-parallel diode is modified such that the peak-to-peak value of v_d matches that of estimated current v_{ec} for each PLL steering logic implementations.

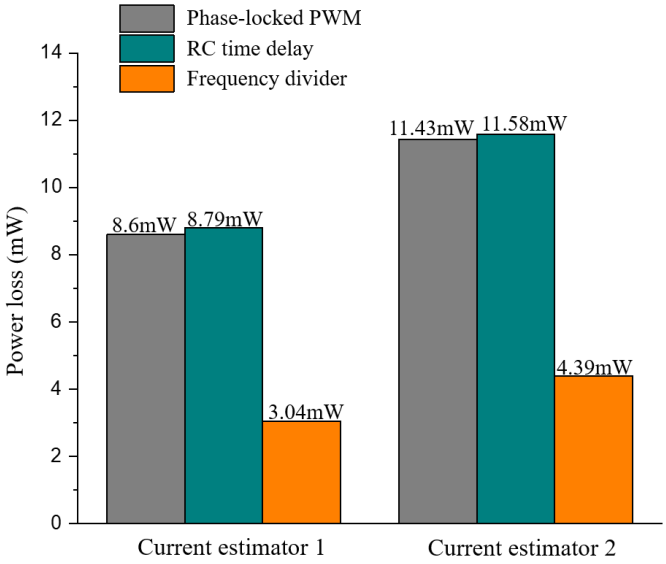

Fig. 14. Power loss comparison of current estimator 1 (CE1) and current estimator 2 (CE2).

As can be seen in Fig. 14, the frequency divider controller shows the lowest power loss amongst those three controllers, with 3.04mW for CE1 and 4.39mW for CE2. The RC time delay controller gives the largest power consumption with 8.79mW and 11.58mW for CE1 and CE2, respectively. These results neglect the power loss in the PLL or logic gates, but those are likely to be similar for all implementations.

Even though the resonant current flow through the circuit with CE1 and CE2 is almost the same, the anti-parallel diodes in CE2 require nearly 0.9V to be fully turned on in practice. In contrast, the sensing resistors R_A and R_B in Fig. 4 provide

relatively small sensing voltages v_1 and v_2 to indicate the zero-crossing points as shown in Fig. 5. Therefore, CE2 consumes more power than CE1 for practical implementation.

2) System initialisation time

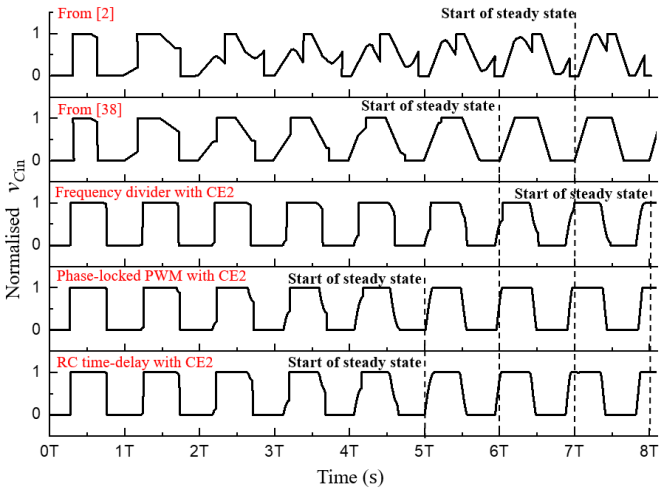

Fig. 15. Comparison of system initialisation time: top plot from [2], second top plot from [39], bottom three plots from frequency divider, phase-locked PWM or RC time delay control respectively using CE2

The system initialisation time of the proposed control method using phase-locked PWM, RC time-delay or frequency divider together with CE2 is compared with previous art and shown in Fig. 15. In this simulation test, we implemented each solution in SPICE without noise. To ensure a fair comparison, the time scale is presented in terms of switching period, and v_{Cin} is normalised to unity.

In Fig. 15, the top plot shows the start-up period of a fixed deadtime control presented in [2]. Seven cycles are required for the switching voltage to reach the positive rail during a single deadtime whereafter the system reaches steady state. The second plot from top shows a dynamically-adjusted control design presented in [39] with six cycles required to reach V_{dc} in a single deadtime.

The proposed method using the phase-locked PWM or RC time delay logic with anti-parallel diode current estimator, shown in the bottom plot, show improved performance in terms of reaching the steady state with a reduced lock-on period. Five cycles enables the PT input voltage to meet the positive rail in a single deadtime. For [2] and [39], the optimum deadtime is detected in each resonant cycle and a total feedback loop phase angle of integer multiple of 2π is satisfied, therefore dynamic phase compensation is necessary every time the resonant frequency changes which is not desirable for fast-tracking.

The proposed methods show the best performance since, during the system start-up, the VCO initially works at its minimum frequency, which is set to be near the resonant frequency. Thus, the PT should be excited and operated in the resonant modes more quickly. For a practical implementation of the PT-based converter control, when changes in optimum operating frequency caused by load and temperature variation are considered, our method is more advantageous since the PLL controller is able to lock on to the optimum frequency irrespective of operating conditions and temperature effects. Fewer lock-on periods enable fast tracking of the optimum frequency thereby improving the overall system efficiency. In addition, both phase-locked PWM and RC time delay implementations require five cycles to reach the steady state, performing better than frequency divider approach which requires eight cycles.

In terms of flexible control of deadtime, the phase-locked PWM and RC time delay approaches also perform better than the frequency divider approach. This is highly desirable when output voltage regulation is required for a practical implementation of a PT-based power supply. Approaches for regulating output voltage reported in the literature include: employing a hysteresis controller [6]; operating frequency modulation (thereby changing the reactance of the resonant tank) [40]; and, adjusting the deadtime [14][39] (hence the duty cycle).

Reference [41] indicates that it is difficult to regulate the output voltage while achieving ZVS with deadtime control and frequency control simultaneously. The proposed phase-locked PWM and RC time delay approaches show potential advantages for a simple and flexible deadtime control to regulate the output since the deadtime interval can be controlled both symmetrically and asymmetrically by adjusting the reference voltages.

The overall performance of all control six approaches are summarised in table I. The choice of control approach must be taken holistically, bearing in mind need for flexibility, noise immunity, system complexity and tracking speed.

TABLE I
SUMMARY OF DIFFERENT CONTROL APPROACHES

	Phase locked PWM		RC time delay		Frequency divider	
	CS1	CS2	CS1	CS2	CS1	CS2
Flexibility	Symmetrical and adjustable deadtime		Symmetrical, asymmetrical adjustable deadtime		Fixed deadtime	
Start-up time	5 cycles		5 cycles		8 cycles	
VCO range	10kHz		10kHz		40kHz	
Maximum circuit noise tolerance (W)	0.09	0.16	0.11	0.17	0.36	0.50
Number of lock-on cycles at maximum noise level	139.79	124.26	110.14	93.19	224.51	190.62
Power loss(mW)	8.6	11.43	8.79	11.58	3.04	4.39

Although the control circuit presented was designed for PT-based inductorless resonant converters, the findings are likely to be generally applicable to other resonant converters [25][42][43], because this approach provides precise phase detection, wide frequency-locking range, adjustable deadtime, small time delay and ease of implementation.

V. Conclusions

A PLL-based control system for achieving ZVS operation in a PT-based resonant power supply was presented. The cooperation between current estimation circuits and PLL controller feedback design were described in detail. By measuring the zero-crossing points of the estimated current, the switching waveforms are locked on to the resonant current while simultaneously ensuring $\pi/2$ radians dead time and hence achieving zero-voltage switching for all loads. The control system is implemented using different current estimation circuits with steering logic and gate signal generators based on CD4046 PLL. A PT emulator with a matched resistive load was used and both simulation and experimental results demonstrate successful ZVS operation. Six implementations were presented and evaluated, each with its own advantages in terms of flexibility, circuit noise condition, power consumption and lock-on time. The phase-locked PWM and RC time-delay approaches show excellent system initialisation performance with only five cycles required to achieve steady state. This ensures a fast-tracking of resonant frequency change. Frequency divider control performs better at circuit noise immunity and has potential advantages for high frequency operation. In addition, CE2 experiences shorter lock-on time under noise conditions and has higher circuit noise tolerance.

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