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MPSOCS FOR RECONFIGURABLE MODULAR SPACECRAFT

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Modular, reconfigurable spacecraft offer a new approach to extending mission capability and maximising the lifetime of a spacecraft. Future uses of space robotics such as in-orbit construction and servicing allow faulty or obsolete parts of a modular spacecraft to be replaced by servicer spacecraft that dock with their targets and perform upgrades and maintenance. Such manoeuvres will require a high degree of autonomy from both platforms and thus will need to leverage high-performance onboard computing for both the robotic control and manipulation of service spacecraft but also for managing

Thales Alenia Space in the UK (TAS UK) and The University of York (UoY) are involved in projects towards this goal and are collaborating to research autonomous network reconfiguration and fault tolerance of the onboard network based on existing space technology (SpaceWire, SpaceFibre). Both organisations have identified FPGA based MPSoCs as a solution for providing the high-performance computing that autonomous robotic systems require, using the FPGA fabric for mission-phase related hardware accelerators (e.g. vision soft co-processors) that can be swapped as the construction or maintenance task demands.

In this presentation we will describe the modular spacecraft avionics unit that TAS UK is developing for the H2020 MOSAR project. This is based on the Xilinx Ultrascale+ MPSoC and uses the “big-little” architecture to provide a split between the spacecraft module’s mission functionality (executing on the “big” quad-core A53) and the support functions to provide: the communication network, module-to-module docking management and the module power management functions of the spacecraft (implemented on the “little” dual-core R5 cores).

Details on our development of an AXI4 compatible SpaceWire and RMAP IP core will also be included. RMAP forms an important part of the MOSAR fault management strategy and this core allows processor-transparent RMAP access to the full MPSoC address range, with automatic DMA descriptors for all other SpaceWire traffic. The AXI4 interface simply allows it to be dropped into any Ultrascale+, Zynq 7000 and NG-ultra based design and several configuration options allow options such as SpW front end type (oversampling /clock recovery) and output data path width (32-bit/16bit) to be selected.

We will also present details of research by the University of York on using RMAP in a MPSoC environment. Access to the full address space of a MPSoC via RMAP brings security and fault management concerns to complex SoCs and hardware security based approaches (e.g. ARM’s TrustZone) could be used in future MP-SoC architectures to protect against damage by either corrupt RMAP packets, damage from failure modes of RMAP initiators or malicious/compromised spacecraft modules. To tackle autonomy challenges UoY is currently developing a reasoner based, reconfigurable modular robotic platform that can cope with uncertain environments that arise in space applications using FPGA based MPSoC and soft-processor technologies.

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