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Single-Chip Reduced-Wire CMUT-on-CMOS System for Intracardiac Echocardiography

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***Abstract*—CMUT-on-CMOS integration is particularly suitable for catheter based ultrasound imaging applications, where electronics integration enables multiplexing capabilities to reduce the number of electrical connections leading to smaller catheter cable profiles. Here, a single-chip CMUT-on-CMOS system for intracardiac echocardiography (ICE) is presented. In this system, a 64 element 1-D CMUT array is fabricated over an application specific integrated circuit (ASIC) that features a programmable transmit beamformer with high voltage (HV) pulsers and receive circuits using 8:1 time division multiplexing (TDM). Integration of pitch matched 64 channel front-end circuits with CMUT arrays in a single-chip configuration allows for implementation of catheter probes with miniaturization, reduced number of cables, and better mechanical flexibility. The ASIC is implemented in 60 V 0.18 µm HV process. It occupies 2.6×11 mm^2 which can fit in the catheter size of 9F, and reduces the number of wires from more than 64 to 22. This system is used for B-mode imaging of imaging phantoms and its potential application for 2D CMUT-on-CMOS arrays is discussed.**

Keywords— Capacitive micromachined ultrasound transducer (CMUT), medical ultrasound imaging, intracardiac echocardiography (ICE), CMUT-on-CMOS.

I. Introduction

One of the important advantages of Capacitive micromachined ultrasound transducer (CMUT) technology is the ease of electronics integration which is particularly important for catheter based imaging such as intracardiac echocardiography (ICE) and intravascular ultrasound (IVUS) [1]. Using a low temperature fabrication process, CMUT arrays can be fabricated directly on CMOS wafers containing the imaging electronics to realize a single chip imaging system [2], [3]. This compact single chip integration approach can provide less complex and lower cost catheter structures as compared to piezoelectric transducer-on-CMOS integration [4].

Current commercial ICE catheters have limitations of large number of interconnections, since each channel element of transducer requires a separate connection to external ultrasound system. This is a barrier to improve the image quality by limiting the number of elements. Also for utilizing ICE catheters during magnetic resonance imaging (MRI), the interconnection number should be minimized to reduce RF-induced heating of the conducting lines [5], [6]. Furthermore,

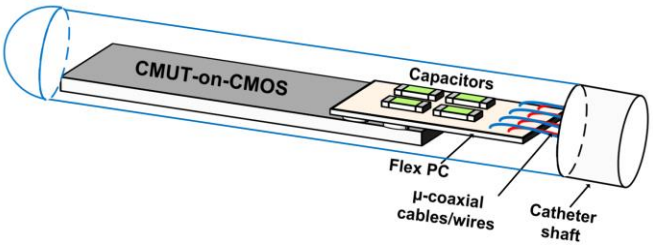

Fig. 1. Schematic drawing of the ICE catheter tip using a single chip CMUT-on-CMOS system. The chip would be connected to the catheter cables using an interposer.

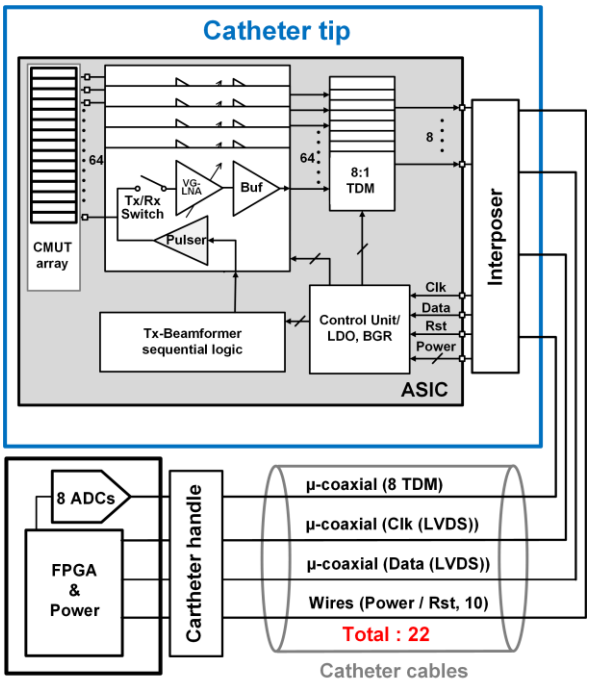

Fig. 2. Simplified block diagram of the proposed CMUT-on-CMOS system.

cable reduction is required to implement 3D ICE imaging using 2D transducer arrays [4].

In this paper, the CMUT-on-CMOS based ICE imaging concept is demonstrated on a 64 element array designed for 2D ICE imaging. Cable reduction on the transmit (Tx) side is achieved by integrating a fully programmable Tx beamformer,

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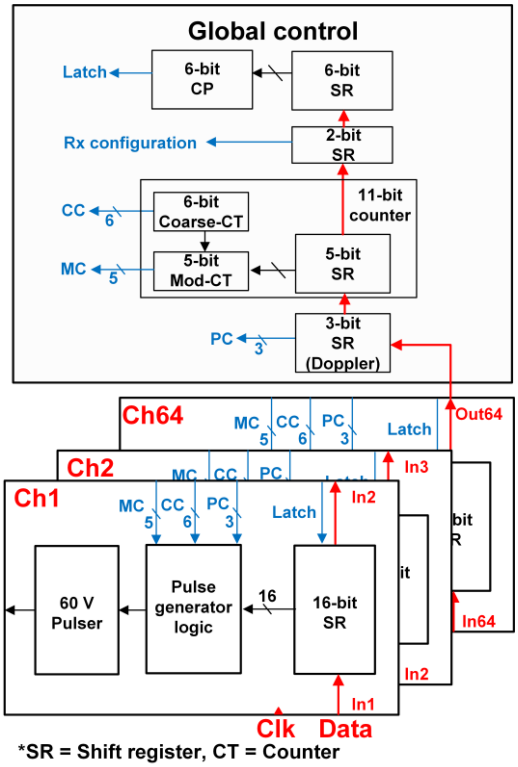


Fig. 3. Simplified block diagram of the Tx beamformer with Pulser.

whereas 8:1 time division multiplexing (TDM) is used on the receive (Rx) side. This approach allows access to raw channel data so that imaging performance is not compromised, and the Tx and Rx apertures are matched with each element having a dedicated high voltage (HV) pulser for best lateral resolution [7]. The proposed catheter tip structure is schematically shown in Fig. 1. With reduced number of cables, this approach would yield a mechanically flexible catheter which can potentially be cooled when used under MRI. This paper is organized as follows. Section II describes the system architecture and ASIC level operation of Tx/Rx. Section III describes the CMUT design and fabrication. The electrical and acoustic measurements are presented in Section IV before concluding in Section IV.

II. ASIC System Achitecture

The proposed system aims to reduce the number of wires at the catheter tip by implementing Tx beamformer and Rx TDM circuits in a single-chip for ICE application. Fig. 2 shows the simplified block diagram of the proposed ICE system. Each of 64 CMUT elements is driven by a HV pulser, which can generate 60 V unipolar pulse. The beamforming profile can be loaded during each firing to steer and focus ultrasound beam over the desired ±45° field of view with a single low-voltage differential signaling (LVDS) data line. A Tx/Rx switch protects low voltage (LV) circuits from HV pulser during Tx operation period. Variable gain low noise amplifier (VG-LNA) compensates for the attenuation of reflected echo signal by adjusting gain at 4 levels to implement simple time gain compensation (TGC), which does not require extra TGC circuits in addition to LNA. The TDM circuitry reduces the number of output signals from 64 to 8, and the high frequency (HF) buffers drive the TDM signals to catheter handle. After that, the TDM signals are delivered through Ethernet cables to the backend system. The ADC in the backend system samples the corresponding channel at the right time to implement direct digital demodulation (DDD) [8]. The CMUT array is directly fabricated on top of the ASIC as shown in Fig. 1, and the interposer is placed at the end of the chip with pads to connect the ASIC with μ-coaxial cables and wires to the catheter. The catheter cables consists of a µ-coaxial cables for 200 MHz of clock, data, and TDM output signals and single wires for power, bias and control lines. The received multiplexed echo signals are delivered through catheter handle to ADCs in the backend system, where DDD is performed in the FPGA for advanced imaging processing in the digital domain [9].

The backend system consists of a power supply module which has AC-DC converter, DC-DC converters, an FPGA board, an ADC board to support 8:1 TDM system, and PCI express interface to deliver data from FPGA to a computer via an optical fiber, to provide MRI compatibility.

A. *Tx Beamformer Operation*

Tx beamformer is designed to reduce the number of cables by implementing serial-in parallel-out (SIPO) shift registers for each of the 64 channel, which only one LVDS data line is required to load the data. It creates a maximum delay of 10.235 μs with a resolution of 5 ns, which enables the desired view angle of ±45°. This beamformer features pulse-width apodization, so that each Tx element can be driven with a different pulse width [10]. Also for pulsed wave Doppler operation, the beamformer can create multiple pulses up to 8, for narrow band and higher signal-to-noise ratio (SNR) operation. Fig. 3 shows the simplified block diagram of Tx beamformer with pulser. In global control logic block, 6-bit of course counter (CC) and 5-bit of mod counter (MC) generate the control information that the shift registers of each channel can determine the exact delay, pulse width, and number of pulses for each channel, respectively. Each of the 64 channels has 16-bit SIPO shift register that stores beamforming profiles. Once the data is loaded properly, the latch signal locks the shift registers and the counters start to count for pulse generation. It also includes a 2-bit shift register for Rx gain control configuration, since the beamformer knows the timing of TGC control. To program the delay profile for all the channels, each programming cycle requires a 1040-bit data packet, which corresponds to 5.2 μs. All the registers are reset before programming Tx beamformer, and the data packet is generated and sent from the FPGA from backend system.

B. *Rx Circuitry*

As shown in Fig. 2, 64 channels of Rx circuitry consist of Tx/Rx switch, VG-LNA, buffer, and TDM circuitry. The LNA is designed to have 4 different gain stages (15 dB, 21 dB, 27 dB, and 32 dB) to meet the dynamic range of ADC in the backend system with the assumed input echo signal dynamic range of 76 dB. Rx front-end topology in ultrasound system

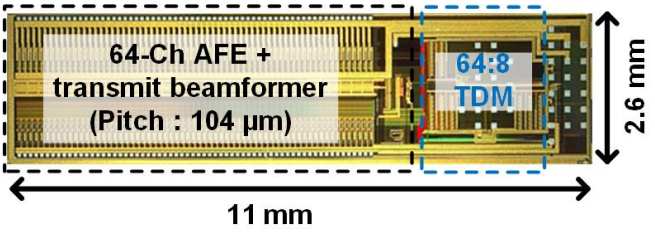


Fig. 4. Microphotograph of the ASIC.

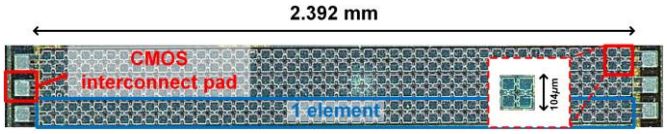


Fig. 5. Microphotograph of the membranes of 1D CMUT-on-CMOS elements.

usually depends on the electrical impedance of transducer type. The transimpedance amplifier (TIA) is a commonly used topology in CMUT because the equivalent electrical model of CMUT is comparably high impedance. However, for this particular application with comparably large 1D CMUT array elements, the impedance level is low. Therefore a LNA structure is adopted for driving relatively large capacitance (~10 pF) [11].

During the Tx period, the LV circuits should be protected by Tx/Rx switch from HV pulse. After HV pulse generation period, VG-LNA amplifies the echo signals based on the traveling time for compensation, the buffer drives the signal to TDM circuitry. The TDM circuitry samples and combines the output signals with 8:1 ratio to the backend system. The TDM technique allows multiple channels to share the same cable by assigning a corresponding time slot to each channel. Analog TDM requires a relatively simple design and less power because it needs analog multiplexer, digital counting logic which can be shared with Tx beamformer, in addition to sample and hold circuits, which is suitable ICE application. Also in this proposed system, by using DDD technique, ADC could sample TDM output with the same frequency. This results in less data processing to increase efficiency in the backend system [8]. In this system, the clock frequency is chosen as 200 MHz, resulting in 25 MS/s for each channel of 8:1 TDM circuitry. To reduce the cross-talk level due to inter symbol interference, the HF buffer is designed to have around 400 MHz bandwidth. The TDM circuitry consists of 8 sets of TDM blocks, and each TDM block consists of 8 channels of sample and hold switches. The link training switch is used to optimize the sampling time and identifying the channel numbers. Phase synchronization for the TDM sampling is performed in FPGA of backend system, so that ADC takes samples when the signal through the interconnection has stabilized rather than during the switching transients.

Note that this TDM approach can be combined with well-known subarray beamforming (SAB) techniques as the frequency content of the subarray beam-formed signals is the same as the raw data [12]. This would be particularly useful in 2D arrays where cable reduction is a requirement. With a typical 3x3 subarray, cable reduction ratio of 72:1 can be achieved with using TDM cascaded with SAB. Alternatively, SAB size can be reduced for better imaging performance as TDM will provide the desired overall cable reduction ratio.

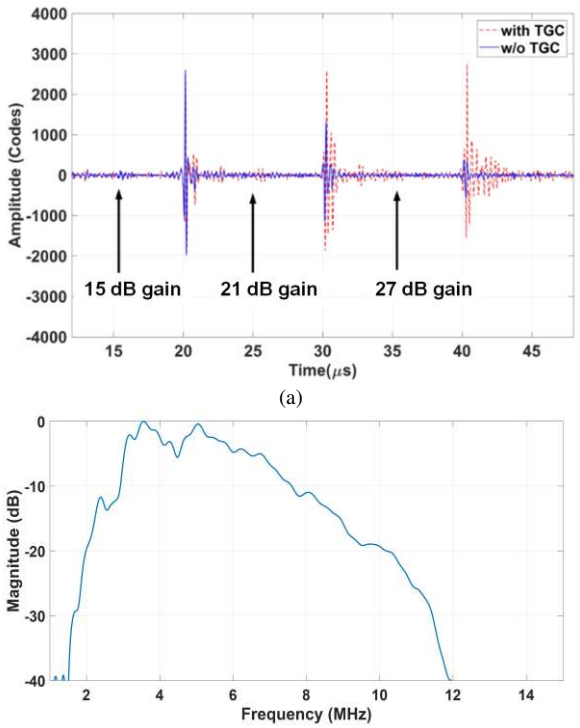
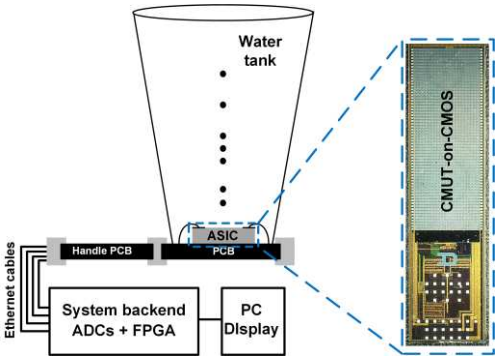


Fig. 6. (a) Received pulse-echo signals with or without TGC, and (b) frequency spectrum of the echo signals from plain reflector.

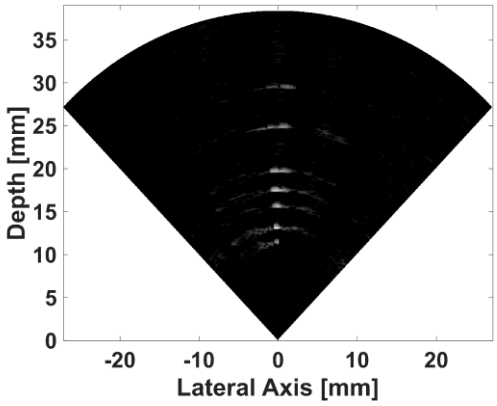
The ASIC for this CMUT-on-CMOS system is fabricated in a 0.18-μm 60 V power management 4M1P HV-BCD CMOS process. It consists of 64 channel AFE (pulser, Tx/Rx switch, LNA, and buffer), Tx beamformer, and symmetrically designed TDM, which occupies 2.6×11 mm^2, as shown in Fig. 4. The pads for power supply, control signals, and TDM outputs are located on the right side, on which an interposer will be bonded to connect μ-coaxial cables and wires.

III. CMUT Design and Fabrication

The CMUT arrays are fabricated using low-temperature CMUT-on-CMOS process [2], [13]. The arrays are processed on the CMOS substrate which is passivated with 3 μm of Plasma-enhanced chemical vapor deposition (PECVD) silicon nitride (SiN). 250 nm of Cr is deposited for bottom electrode, followed by 120 nm of Cu deposition for the sacrificial layer that eventually forms gap height. 250 nm of SiN is then deposited as the isolation layer to ensure that the top and the bottom electrodes do not short during large membrane displacement. 200 nm of AlSi is sputtered on the isolation layer for the top electrode. The SiN is then deposited to form the actual membrane thickness followed by membrane release, etching sacrificial layer, and drying process. Fig. 5 shows the



(a)



(b)

Fig. 7. (a) Imaging experiment setup diagram with micrograph of CMUT-on-CMOS, and (b) B-mode image of 7 metal wires in the water.

micrograph of CMUT membranes. Each of 64 element consists of 92 (2×46) membranes, which shows a pitch of 104 μm with length of 2.392 mm, and each 2 μm thickness membrane occupies 45×45 μm^2.

IV. Experimental Results

Fig. 6(a) shows the pulse echo measurement results in oil using the CMUT-on-CMOS chip. The results are shown with and without applying the TGC gains indicating the functionality of the system. The results show 5 MHz center frequency with 80 % of -6 dB fractional bandwidth (Fig. 6(b)), suitable for ICE catheter imaging. Imaging experiments are also performed using 7 metal wires (38 AWG, 101 μm in diameter). In these experiments, 3 μm Parylene coated CMUT-on-CMOS chip is immersed in the water facing 7 wires vertically as shown in Fig. 7(a). Tx beamformer is programmed to generate 123 focused and steered beams to scan ±45° sector image. The obtained image is shown in Fig. 7(b) with 40 dB of dynamic range, clearly showing the expected details of the imaging target.

V. Conclusion

CMUT-on-CMOS approach is used to implement a single chip, reduced wire ICE imaging system. Cable reduction is achieved by integrating both Tx beamformer and TDM based Rx circuitry in a single chip for a 64 element 2D imaging ICE catheter. The Tx beamformer is capable of steering and focusing the Tx beams in a wide angular range and can be programmed with single LVDS data line. TDM based Rx cable reduction has the potential for integration with other channel count reduction techniques for use in 2D arrays for 3D imaging catheters. The electrical and acoustical experimental results confirm the functionality of the complete system and indicate the potential of the approach for cable count reduction and simple catheter construction leading to lower cost, mechanically flexible ICE catheters with improved image quality and MRI compatibility.

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