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Supply-Inverted Bipolar Pulser and Tx/Rx Switch for CMUTs above the Process Limit for High Pressure Pulse Generation

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Abstract—A combined supply-inverted bipolar pulser and a Tx/Rx switch is proposed to drive capacitive micromachined ultrasonic transducers (CMUTs). The supply-inverted bipolar pulser adopts a bootstrap circuit combined with stacked transistors, which guarantees high voltage (HV) operation above the process limit without lowering device reliability. This circuit generates an output signal with a peak-to-peak voltage that is almost twice the supply level. It generates a bipolar pulse with only positive supply voltages. The Tx/Rx switch adopts a diode-bridge structure with the protection scheme dedicated to this proposed pulser. A proof- of-concept ASIC prototype has been implemented in 0.18-μm HV CMOS/DMOS technology with 60 V devices. Measurement results show that the proposed pulser can safely generate a bipolar pulse of -34.6 to 45 V, from a single 45 V supply voltage. The Tx/Rx switch blocks the HV bipolar pulse, resulting in less than 1.6 V at the input of the receiver. Acoustic measurements are performed connecting the pulser to CMUTs with 2 pF capacitance and 8 MHz center frequency. The variation of acoustic output pressures for different pulse shapes were simulated with the large signal CMUT model and compared with the experimental results for transmit pressure optimization. A potential implementation of the methods using MEMS fabrication methods is also described.

Index Terms—Pulser, capacitive micromachined ultrasound transducer (CMUT), medical ultrasound imaging, Tx/Rx switch, ASIC, large signal model.

I. Introduction

Capacitive micromachined ultrasound transducer (CMUT) has been shown to be a viable alternative to conventional piezoelectric sensors and transducers in ultrasound diagnostic imaging [1], [2], and several commercial probes have been developed [3], [4]. Although wide bandwidth and electronics integration are considered as advantages of CMUTs [5], nonlinear transmit behavior and lower voltage to pressure conversion ratio in Pa/V are cited as the disadvantages [6], [7]. Several methods have been proposed to reduce the CMUT nonlinearity while driving it with large voltages suitable for tissue harmonic and contrast ultrasound imaging [8], [9]. Large displacement (gap) requirements for high transmit pressures lead to smaller CMUT capacitance, limiting the Pa/V sensitivity, and large gap swings result in nonlinearity. Therefore, a viable method to improve the overall CMUT output pressure requires optimized transmit pulse shapes, presented by a large signal model, and utilization of the maximum pulse voltages afforded by the integrated circuit (IC) process without causing damage. An accurate large signal model for non-collapsed CMUTs has been developed for this purpose to perform pulse shape optimization [10], [11]. Recent research has also shown that the optimized bipolar pulse shape suppresses the second harmonic contents, making CMUT probes more useful for harmonic imaging mode applications [12].

Two level high voltage (HV) digital pulsers are commonly used in CMUT ultrasound imaging systems for their simplicity [13]. A three-level pulser with pulse shaping and charge recycling capabilities has also been reported in [14], saving power in the pulser at the cost of requiring multiple supply voltages, requiring HV DC-DC converters and extra capacitors and increasing the overall system complexity. Additionally, it is shown in [15] a differential three level pulser that achieves lower power consumption and area reduction compared to commonly used single ended pulsers. This differential pulser took advantage of the fact that each of the CMUT terminals can be connected to a different pulser obtaining a differential driving voltage. However, it still requires multiple HV supplies.

A motivation for this work is catheter based imaging applications, such as intracardiac echocardiography (ICE) and intravascular ultrasound (IVUS). These applications would benefit from electronics integration at the catheter tip for improved performance. This can also result in improved safety at lower cost by using lower voltages on the catheters without compromising the pulser output voltage levels. One possible

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solution is adopting bootstrapping circuit in the pulser design, which is commonly used in various applications including sample-and-hold circuits in analog-to-digital converters (ADC) [16], [17], and DC-DC converters [18]. These circuits are widely used for generating twice the supply voltage to maximize the efficiency of the circuit or to reduce ON-resistance of the switches. In cases where the CMUT fabrication processes allow HV capacitors to be built within their MEMS structure, these capacitors can be used in the pulser bootstrap circuit to further reduce the size and voltage drop across the long catheter wires by using a lower external supply voltage. Although this approach could also be applied to piezoelectric transducers, bootstrapping circuits requiring extra HV capacitors would be more suitable for CMUT based catheters that utilize CMUT-on-CMOS or flip chip bonded CMOS electronics [19], [20]. A supply-doubled pulser using a bootstrapping circuit for driving CMUT was proposed in [21], which showed pulse-shaping capability with a single HV supply. However, in that example, it was limited to a positive unipolar pulse, and lacked a protection HV switch, prohibiting the use of the same CMUT element both for transmission and for reception.

In this paper, a HV supply-inverted bipolar pulser combined with a Tx/Rx switch is presented. The pulser provides a HV output swing close to twice its supply voltage, and above the device breakdown, which is often limited by the CMOS fabrication process. The design and operation of the pulser and Tx/Rx switch circuit topologies for an intracardiac ultrasound imaging catheter application is described in detail in Section II. Experimental results obtained using a CMUT are compared with simulations using a large signal nonlinear model to validate the experimental results in section III.

II. High Voltage Pulser And Tx/Rx Switch Design

A. Circuit topology

The design goal of the supply-inverted pulser is to generate a bipolar pulse with peak-to-peak amplitude close to twice the supply voltage without requiring a negative HV supply. It is important that every circuit element is within safe operating range, including receiver's low voltage (LV) devices during the supply-inverting operation. Fig. 1a illustrates a simplified schematic diagram of the proposed pulser and Tx/Rx switch. The digital control logic from external pulse generators trigger low voltage control signals to drive N-type double-diffused metal oxide semi-conductor (DMOS) transistors to turn on/off low side switches. The level shifters convert the DC voltage levels of control signals to drive P-type DMOS transistors of the pulser to control high side switches. The Tx/Rx switch protects the low voltage receiver from HV signals including the negative part of the HV pulse. Blocking this negative HV pulse requires careful design as the output drops lower than the substrate voltage, which can cause parasitic diodes to switch on unexpectedly.

Fig. 1b illustrates operation of the voltage inverting stage. A capacitor, C, which can be on-chip or integrated with the CMUT array, is charged to $-HV_{DD}$ during negative charging

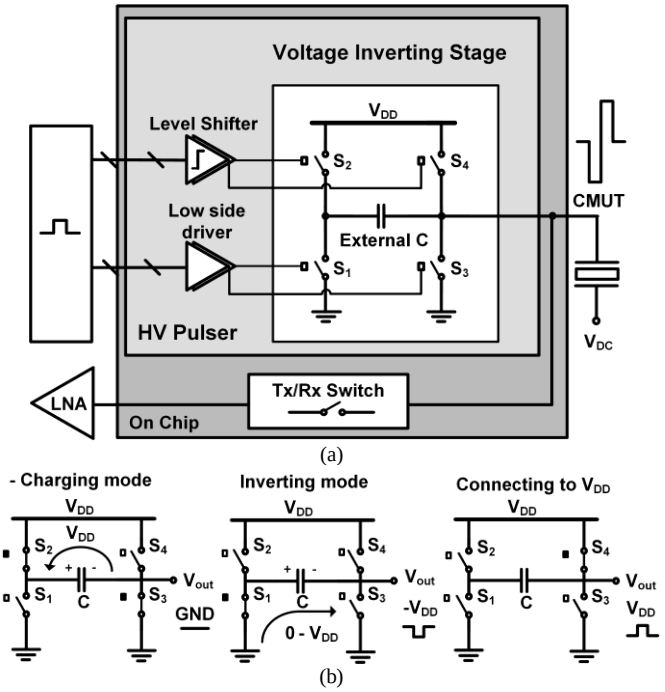


Fig. 1. (a) Simplified schematic diagram of the proposed pulser and high voltage Tx/Rx switch, (b) the operation of voltage inverting stage.

mode through S_2 and S_3. During this negative charging mode, V_{out} is still at ground. After C is fully charged, then a HV switch, S_1, drives the positive terminal of C to GND during inverting mode, while all other switches are open, resulting in V_{out} reaching $-HV_{DD}$.

The CMUT can be regarded as a capacitive load, resulting in a capacitive voltage divider between C and the CMUT. The actual output pulse voltage level is described in more detail in section II.B. All these circuits require careful design because they go beyond the safe operating voltage. To ensure safe operation, stacked transistors, protection Zener diodes, and Schottky diodes are utilized to prevent any transistor from operating outside of its rated specifications.

B. Design and operation of voltage-inverting pulser

Fig. 2 shows a detailed schematic of the supply-inverted bipolar pulser, controlled by three 1.8 V input control signals (I_1, I_2, and I_3). These signals can be generated by on-chip control logic or an off-chip field-programmable gate array (FPGA). The N-type DMOS transistors, M_1 and M_3, are driven by 0 - 5 V control signals, while P-type DMOS transistors, M_2, M_4, and M_5, are driven by level-shifted HV control signals (note that in this case, HV_{DD} = 45 V). Because of the large size of DMOS transistors, level shifters are designed as simple as possible, ensuring that I_{P1} and I_{P2} generate 40 – 45 V sharp pulses with small current consumption, compared to the CMUT driving stage, as shown in Fig. 2b [22]. The control signals for N-type DMOS transistors have the additional buffers to optimize the delay difference between P-type and N-type DMOS transistors. M_4, is driven by level-shifted 0 – 40 V control signal, I_{P3}, which ensures turning on M_4 when M_5 is on and protecting M_5 from the drain-source junction breakdown when V_{out} is negative.

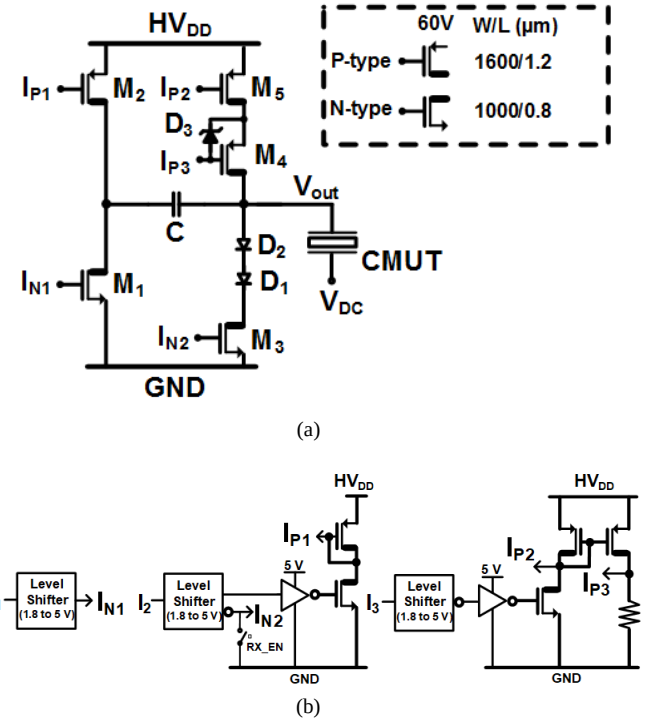


Fig. 2. Schematic diagrams of (a) proposed supply-inverted pulser, (b) simplified level shifters for high voltage NMOS/PMOS input signals of supply-inverted pulser.

The circuit operation is similar to the bootstrapping circuits in [16], [17]. During negative charging mode, C is charged to HV_{DD} - (V_{D1} + V_{D2}) by turning on M_2 and M_3 transistors, where (V_{D1} + V_{D2}) is the forward voltage drop across D_1 and D_2. When C is fully charged, turning on M_1 and turning off all the other transistors drives V_{out} to a negative voltage of -HV_{DD} + (V_{D1} + V_{D2}). During this inverting period, it is crucial to ensure that all devices in the circuit are within the safe operating limits, considering the fact that in this process, the drain-source junction breakdown and gate-oxide breakdown voltages are 60 V and 5 V, respectively. To prevent N-type M_3 from negative V_{DS}, two HV Schottky diodes, each of which can handle a maximum reverse voltage of 36 V, are added in series with M_3. When the output is inverted, these two diodes should handle 45 V of total reverse voltage between them, resulting in each diode having reverse voltage well below its limit. Two P-type M_4 and M_5 are stacked to ensure safe operation when V_{out} is inverted. The gate of M_4 is biased to 0 V during inverting period, while the Zener diode, D_3, keeps V_{GS} of M_4 below 5 V, so that M_4 and M_5 can divide ~2HV_{DD} across their designated drain-source voltage limit. In order to eliminate latch-up and turn-on of parasitic effects, every DMOS transistors have separate guard rings which is very close to the transistors. Also during the simulations, parasitic diodes of DMOS transistors and diodes which the P-type and N-type wells connecting the device to the substrate are considered for modeling the real silicon situation.

$$V_C = HV_{DD} - (V_{D1} + V_{D2}), \quad (1)$$

$$V_{out} = -V_C \times \frac{C}{C + C_{CMUT}}, \quad (2)$$

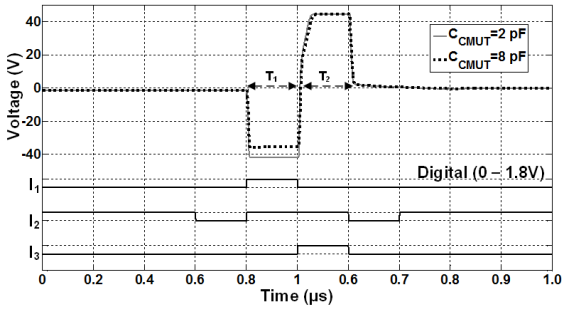


Fig. 3. Simulation of the output pulse with different C_{CMUT} values with 30 pF of C.

The value of C is a key factor in determining the inverted voltage of V_{out} as shown in equations (1) and (2), where C_{CMUT} is the equivalent capacitance of the CMUT. To achieve V_{out} ≈ -HV_{DD}, we need C >> C_{CMUT}. However, large C increases the RC time constant of the output during negative charging mode, limiting the operating frequency range and slew rate as in equation (3), where $I_{max\_negative}$ is the maximum current sourced to C from P-type forward-biased M_2, which mainly depends on the size of driving DMOS transistors.

$$SR_{negative} = \max\left(\frac{dV}{dt}\right) = \frac{I_{max\_negative}}{C}, \quad (3)$$

It should also be noted that if C is integrated in the CMUT, its value may be limited by the size of the CMUT, thus deciding the optimal value of C is a key step the design of this supply-inverted pulser.

If we generate a bipolar pulse by firing the supply-inverted pulse first and positive pulse next, as shown in Fig. 3, a negative charging period happens before the firing, when V_{out} is at GND. This time could be set to fully charge C before firing, such that the slew rate during the negative charging mode would not be an issue which is shown in (3). The supply-inverted pulse is generated by simply connecting the negatively charged C in series with C_{CMUT}, in which case the output pulse voltage can be calculated as per equations (1) and (2). The pulse faces slow charging issue when V_{out} needs to reach HV_{DD} during the positive pulse generation, at which moment, M_1 and M_2 are turned off, and M_4 and M_5 are on. In the first part of this transition, when V_{out} increases from -HV_{DD} to GND, the voltage at the common drain of M_1 and M_2 goes from GND to HV_{DD}, because the charged capacitor drives this node at HV_{DD} above V_{out}. This transition happens rapidly because the positive side of C, which is connected to the drain of M_1 and M_2, is floating. However, in the second part, when V_{out} is going above GND, the positive side of C tries to go over HV_{DD}, which results in reverse current in M_2 due to the negative V_{SD} over this P-type DMOS, which is limited to around -0.7 V in this fabrication process. Therefore, reverse-biased M_2 connects the positive side of C to HV_{DD}, in parallel with C_{CMUT}, which is itself connected to another DC supply, V_{DC}. The slew rate of V_{out} rising edge when it goes above GND is derived from equation (4), where $I_{max\_positive}$ is the maximum current of P-type M_5, which is partly flowing through C and reverse-biased M_2 in series, and partly through C_{CMUT}. This indicates that larger

values of C could limit the rising edge slew rate during the positive V_{out} transition. Therefore, the value of C is a key factor that affects the pulser operating frequency.

$$SR_{positive} = \max\left(\frac{dV}{dt}\right) = \frac{I_{max\_positive}}{C + C_{CMUT}}, \quad (4)$$

In this prototype, we have considered the bipolar pulser for the application of driving a 2-D CMUT array in intracardiac echocardiography (ICE) with 8 MHz center frequency. The CMUT array element size is limited to 100 × 100 μm^2, resulting in C_{CMUT} to be in the order of 2 pF. A realistic design target for the pulser would be to achieve negative peak HV level of at least -0.8 × HV_{DD}, with a rise time shorter than a quarter of the CMUT center frequency period, i.e. 31.25 ns for 8 MHz. According to (1) and (2), the minimum required C would be larger than 4×C_{CMUT}. Considering the forward voltage drop across the diodes and parasitic capacitances of the large DMOS transistors, we chose C = 30 pF for 2 pF of C_{CMUT}. Also to obtain SR > 3 V/ns during the charging mode, M_5 is designed to have I_{max} > 100 mA, based on (4). Since the size of large DMOS transistors mainly determine the layout size, $I_{max\text{-}positive}$ is chosen for driving a 2 pF CMUT load at 8 MHz operating center frequency. However, we also investigated the case for an 8 pF CMUT capacitance, represented by an oscilloscope probe (P6139A, Tektronix) in our characterization.

To verify the pulser design and compare with measurements, the voltage-inverted output pulse was simulated for 2 pF of CMUT load and 8 pF of passive probe loading, for which C = 30 pF, as in Fig. 3. With 2 pF load, simulations show V_{out} with 86.2 V_{pp}, 3.9 ns of first fall time, 25 ns of rise time, and 5.5 ns of second fall time, which is suitable for driving a CMUT array with 8 MHz center frequency. With 8 pF load, simulations show output pulses with 80.3 V_{pp}, 4.3 ns of first fall time, 31 ns of rise time, and 6 ns of second fall time. Note that in Fig. 3, the pulser operation begins from 0.6 μs by charging C. By controlling I_1, I_2, and I_3, the pulse shape and duty cycle of the output pulse can be fine-tuned to generate bipolar pulses with optimal shape that would maximize the acoustic pressure generated by the CMUT.

C. Design and operation of Tx/Rx switch

The Tx/Rx switch located between HV pulser and LV receiver, toggles between transmit and receive mode to prevent HV pulses from damaging the LV receiver circuits. This is a critical circuit in highly integrated ultrasound imaging systems when the ultrasound pulse transmitting and echo receiving circuits interface with the same CMUT element. Since the proposed supply-inverted pulser generates negative HV pulse, which is lower than the ASIC substrate voltage, the Tx/Rx switch requires a careful protection scheme. Conventional Tx/Rx switches consist of two NMOS transistors requiring several level shifted control signals and both positive and negative HV supplies to block HV bipolar pulse during Tx mode [23]. This approach increases the design complexity. The proposed Tx/Rx switch does not need extra level shifted control signals and protects the LV circuits without dual HV supplies, simplifying the design, as a result.

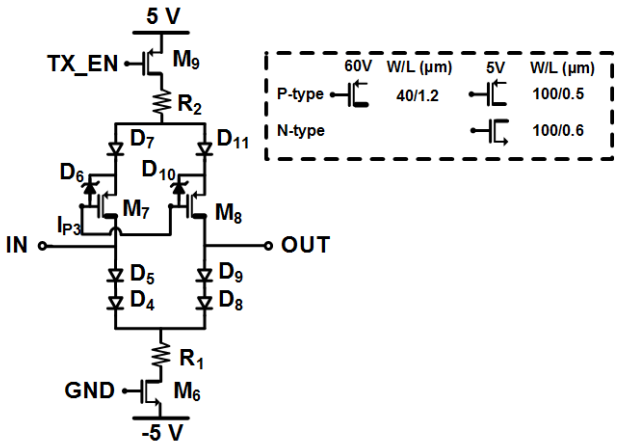


Fig. 4. Schematics of proposed protection Tx/Rx switch for voltage-inverted pulser.

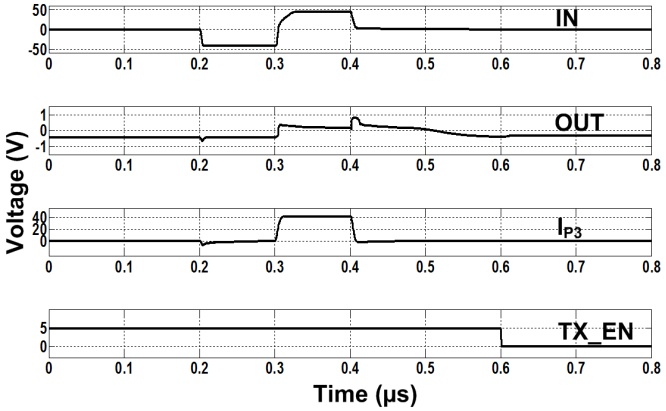


Fig. 5. Simulation result of the Tx/Rx switch, IN is connected to the output of supply-inverted pulser during Tx period.

The proposed Tx/Rx switch schematic is shown in Fig.4, which consists of a diode-bridge, biasing current sources, and clamp diodes, similar to off-the-shelf ultrasound switches [24], [25]. However, it also includes P-type DMOS transistors, M_7 and M_8, each with a Zener diode for negative HV pulse protection. All diodes in this design are HV Schottky diodes except for D_6 and D_{10}, which are protection Zener diodes. The two paths of the diode-bridge are symmetrical for balancing the current. The switch requires 2 control signals, one of which is TX_EN that goes from 0 V to 5 V during Tx HV pulse generation, and the other one, I_{P3}, is the same control signal that is also used in the supply-inverted pulser in Fig. 2.

To turn off the Tx/Rx switch to block the HV bipolar pulse, TX_EN, which is at 5 V, turns off M_9, which in turn shuts down the Tx/Rx switch. During this period, all transistors are off, and the input side of the Tx/Rx switch does not load the supply-inverted pulser. The power down period can be divided into two conditions, when the input is a negative HV pulse and when it is a positive HV pulse. During the negative HV pulse, I_{P3} = 0 V, which turns M_7 off, while D_6 keeps it in the safe operating region. HV Schottky diodes, D_4 and D_5, can divide 45 V of total reverse voltage between them, resulting in each diode having reverse voltage well below its breakdown limit. It should be noted that without M_7, the negative pulse would turn

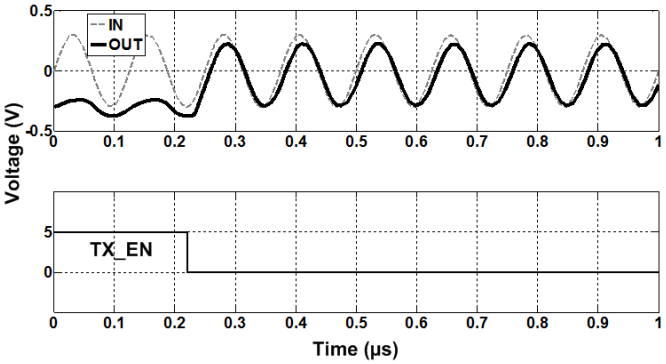


Fig. 6. Simulation results of the Tx/Rx switch with 8 MHz of sinusoidal input. The load condition of the output node is 5 pF.

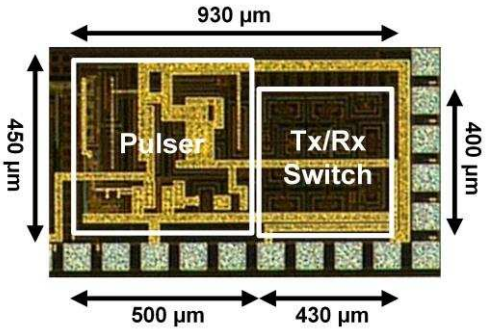


Fig. 7. Microphotograph of the proposed supply-inverted pulser and Tx/Rx switch.

on D_7, and affect the output HV pulse by lowering the impedance. During the positive HV pulse, I_{P3} = 40 V, which keeps M_7 in the safe operating region by limiting V_{SG} of M_7 to be less than 5 V. D_4 and D_5 pass the positive HV pulse to R_1 to reach HV_{DD} - (V_{D4} + V_{D5}), where (V_{D4} + V_{D5}) is the forward voltage drop across D_4 and D_5. D_8 and D_9 can divide 45 V of total reverse voltage between them, resulting in almost 0 V at the output of the Tx/Rx switch. Fig. 5 shows post-layout simulation of the Tx/Rx switch operation, showing that 86.2 V_{pp} of bipolar pulse at the input of the switch is blocked and limited to only 0.8 V at the switch output during Tx period.

To turn on the Tx/Rx switch to pass through the received echo signal, TX_EN is pulled down to turn on M_9. At this moment, the external C would not affect the input loading of the Rx path, because M_1 and M_2 in Fig. 2a are turned off, floating one side of C. We designed the Tx/Rx switch assuming that a high input impedance voltage amplifier stage follows this circuit [26], with the load condition of 5 pF, including the interconnection and amplifier input impedance. The transistor sizes of M_6 and M_9 are selected considering the static current of 288 μA during Rx period, layout size, and ON-resistanceof the Tx/Rx switch. Depending on the type of amplifier, such as resistive feedback or capacitive feedback (low input impedance stage), the optimal size of transistors could be different [27]. Fig. 6 shows simulation result of the Tx/Rx switch with 0.6 V_{pp} sinusoidal input at 8 MHz, achieving -0.8 dB of insertion loss at 8 MHz.

III. Experimental Results and Discussion

The proposed pulser and Tx/Rx switch were fabricated using a 0.18-μm 60 V power management 4-metal 1-poly HV-CMOS process, a micrograph of which is shown in Fig. 7. The occupied core area of the supply-inverted pulser and Tx/Rx switch are 0.225 mm^2 and 0.172 mm^2 respectively. The chip is wire-bonded in a QFN package and mounted on a PCB along with the off-chip surface mount capacitor, C. Fig. 8 compares measurement and simulation of the supply-inverted pulser output with C = 30 pF, and C_{CMUT} = 8 pF. With HV_{DD} = 45 V, the output shows -34.6 V negative and 79.6 V peak-to-peak voltages, and slew rates of -3.11 V/ns, 2.18 V/ns, and -2.02 V/ns during the first fall time, rise time, and second fall time, respectively. Measurements from over 10 chips have shown consistent results with V_{out} (mean±std) = 79.03 ± 1.19 V_{pp}, demonstrating the reliability of this HV pulser. The good agreement between simulation and measurements, lead us to extrapolate ~85 V_{pp} of output pulse with 2 pF of CMUT loading, as shown in Fig. 2.

The Tx/Rx switch was also tested together with the supply-inverted pulser. Fig. 9 shows that the switch does not

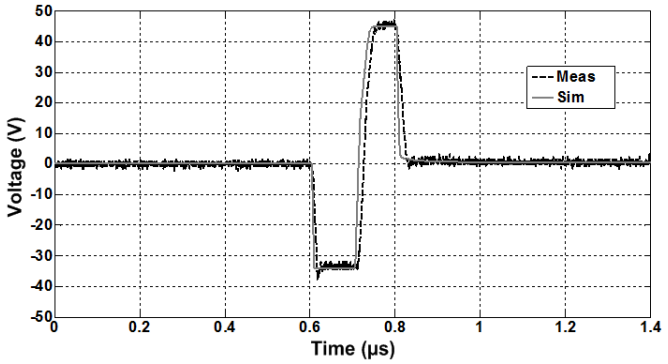


Fig. 8. Measured and simulated supply-inverted output pulse along with three input control signals. C = 30 pF, equivalent C_{CMUT} = 8 pF.

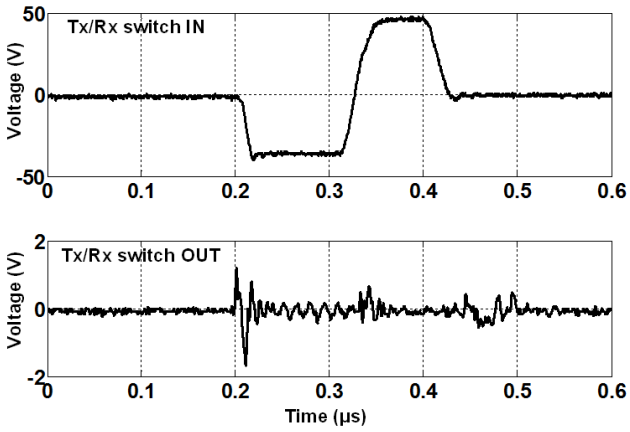
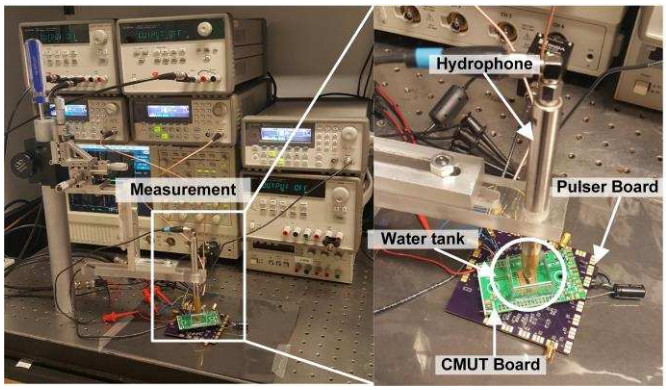


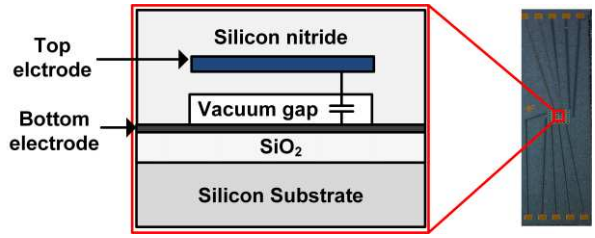
Fig. 9. Measured Tx/Rx switch input and output during supply-inverted pulse firing period. C = 30 pF and equivalent C_{CMUT} = 8 pF.

TABLE I
BENCHMARKING OF THE PROPOSED TX/RX SWITCH PERFORMANCE

Parameter	This work	[23]	[24]	[28]
Supply voltage (V)	±5	±25	±5	±25
Static power (mW)	3	0	90-560	1
Off-isolation (dB)	-28	-53	-40	-90
Limit range (V)	±45	±25	±100	±25
Number of control signals	2	6	3	6
Technology (μm)	0.18	0.18	-	0.35



(a)

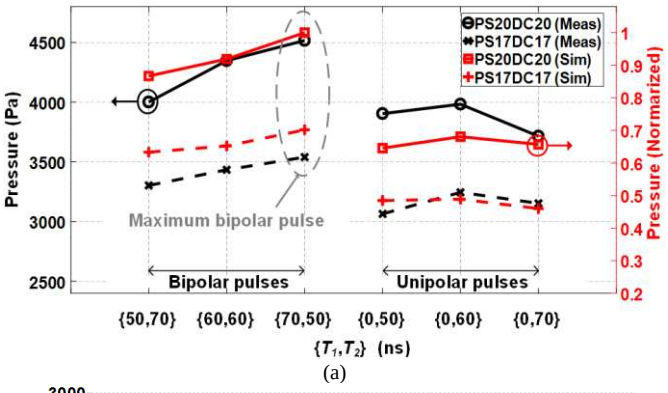


(b)

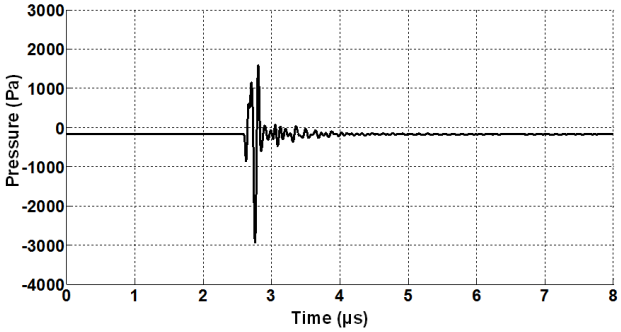
Fig. 10. (a) Experimental setup with CMUT array board and pulser board for acoustic measurements. (b) Cross section view of CMUT layers and layout of the CMUT array which one element consists of 4 membranes.

noticeably affect the output of the supply-inverted pulser during firing, and the HV signal is blocked with only 1.6 V of feedthrough. In this ASIC prototype, the Tx/Rx switch is placed close to the pulser as shown in the Fig. 7 layout, and the HV pulse affects the Tx/Rx switch output through the substrate, creating the spikes shown in Fig. 9 during HV pulser transitions. This can be reduced by placing these design blocks further from one another and adding substrate contacts or shielding between the supply-inverted pulser and the Tx/Rx switch. The overall performance of Tx/Rx switch is benchmarked against prior work in Table I.

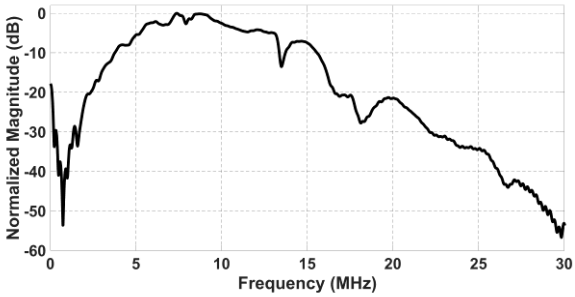
Transmitter acoustic pressure with an actual CMUT load was also measured using a setup shown in Fig. 10. The CMUT used in this experiment was designed for an 8 MHz center frequency and occupied a 100 × 100 μm^2 area on silicon. The element consisted of a 2 × 2 array of four 45-μm wide square membranes, creating a 2 pF element, 1.8 pF of which is the parasitic capacitance due to bond pads. The fabrication was part of a larger 2-D ICE imaging array, fabricated using a low temperature CMOS compatible process [19]. The CMUT array, mounted on a separate PCB and made water resistant by a 3 μm layer of Parylene-C coating, was connected to the larger pulser board via header pins. The off-chip capacitor, C = 30 pF, was selected to obtain maximum output swing, as discussed in section II. The CMUT array was submerged in a water tank, while a hydrophone (HGL-0085, Onda Corp) was positioned directly above the CMUT array, 5.6 mm from its surface, to measure the Tx acoustic pressure. Different pulse shapes were generated to evaluate the impact of the bipolar pulse waveform on the Tx output pressure. The pulse shape is defined by {T_1, T_2}, as shown in Fig. 3. Note that when {0, T_2} is applied, a positive unipolar pulse is generated. The bottom electrode of



(a)



(b)



(c)

Fig. 11. (a) Transmitted peak-to-peak acoustic pressure measurement and simulation with different CMUT bias, pulse shape and supply voltages. (b) Measured transmitted pressure with T_1 = 70 ns, T_2 = 50 ns, HV_{DD} = 20 V, and CMUT bias = 20 V. (c) Frequency spectrum of the transmitted pressure signal shown in Fig. 12b.

CMUT is connected to DC bias, V_{DC}, as shown in Fig. 2a. While using the same CMUT for Tx/Rx operation, a V_{DC} needs to be applied across the CMUT for Rx operation with high sensitivity. V_{DC} of the CMUT was changed from 17 V to 20 V, while HV_{DD} was changed from 17 V to 20 V because the breakdown voltage of the CMUT in these experiments was limited to 40 V. The maximum peak-to-peak pressure of 4517 Pa was measured with {70 ns, 50 ns} of bipolar pulse shape, HV_{DD} = 20 V, and V_{DC} = 20 V (peak- to-peak pulse was ~40 V). Bipolar pulses show larger acoustic pressure compared to positive unipolar pulses, as shown in Fig. 11a, because during the first negative pulse, the potential difference on the CMUT is increased and the gap is further reduced for 70 ns. After the membrane passes through the minimum gap, the positive pulse cancels the DC bias across CMUT and completely releases the membrane for maximum upward gap swing. The unipolar pulse only releases the membrane from fixed gap, which is

TABLE II
BENCHMARKING OF THE PROPOSED PULSER PERFORMANCE

Parameter	This work	[14]	[21]	[22]	[29]
Input voltage (V)	1.8	3.3	5	3.3	1.8
Output voltage (V)	(-)34.6 - 45	0 - 30	0 - 85	0 - 60	0 - 12.8
Supply voltage (V)	45	30	45	60	12.8
Frequency (MHz)	8.33	5	8.33	1.38	1.25
Rise/fall time (ns)	36/11,23	30	26,16/18	68/68	40/50
Power (mW)	35.7	52.4	48.6	98.1	
Power (mA) Dynamic *	170	-	150	-	19.9
Chip area (mm^2)	0.225	-	0.2	0.08	0.022
Output load (pF)	2	40	2	18	15
Bipolar pulse	Y	N	N	N	N
Technology (μm)	0.18	0.18	0.18	0.35	0.18

* Simulation results

determined by V_{DC}, and its upward motion is also resisted by the DC bias. Therefore, a bipolar pulse is expected to generate higher peak pressure [11]. The timing between pulling (T_1) and releasing (T_2) the membrane would also affect the peak pressure. In this measurement, three types of bipolar pulses and three types of unipolar pulses were measured to find the maximum pressure condition. Fig. 11b and Fig. 11c show the time domain transmit signal and its spectrum for the case of maximum pressure, showing a center frequency of 7.8 MHz with -3 dB bandwidth of 4.5 MHz. Fig. 11a also shows the comparison between simulation and measurements, where the simulations are performed using a large signal CMUT model [10], [11]. The comparison with normalized pressures from simulations show good agreement in terms of trends and maxima as a function of pulse parameters for both unipolar and bipolar pulses at different bias voltages. Most of the mismatch comes from the dielectric charging effect in CMUT that degrades the transduction efficiency as the induced polarization reduces the effective bias across the CMUT [30]. In our future work, we will investigate pulse optimization with co-design of the pulser and large signal CMUT model. Table II summarizes specification of the proposed supply-inverted pulser and compares it with previous works. Using positive HV supplies only, the proposed pulser can successfully generate a bipolar pulse above the process limit. Another advantage of this pulser is that without negative HV supply, it can generate a bipolar pulse with a peak-to-peak value surpassing the maximum operating voltage level (60 V in this case) imposed by the process. Therefore, this pulse was able to generate larger acoustic pressure from the CMUT than conventional pulsers that generate a pulse within the supply voltage range.

The multi-level pulsing circuit has advantages in terms of better power efficiency when driving CMUTs [14]. However, it requires several supply voltages or DC-DC converters with large capacitors [31]. Since the capacitors required for DC-DC converters are often quite large, using off-chip components would be inevitable. A potential advantage of the proposed pulser is that, to generate a bipolar pulse, it requires a capacitor that, while it is an order of magnitude larger than C_{CMUT}, can be implemented during microfabrication underneath the CMUT. This is schematically shown in Fig. 12, where a CMUT element is built over a fixed capacitor, C, with approximately the same

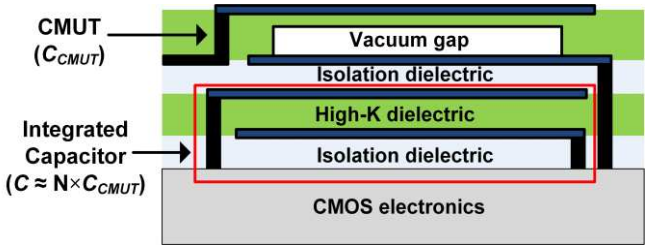


Fig. 12. Schematic cross section view of a CMUT-on-CMOS device with integrated co-microfabricated capacitance, C. Lower relative permittivity dielectric layers (SiNi, SiO_2) are used for isolation, and the high K-dielectric has a relative permittivity of ε_r = N. Black lines are metal connections to the CMOS electronics.

area, and connected to the CMOS electronics using CMUT-on-CMOS technology. While the CMUT capacitor, C_{CMUT}, has a vacuum gap, C is formed by filling a similar gap with a high-K dielectric, such as hafnium dioxide with ε_r = 16. With non-collapsed CMUT operation, one can easily satisfy the required C >> C_{CMUT} condition in this approach, considering that in CMUT-on-CMOS implementation the parasitic capacitance will be minimized. For instance, a breakdown voltage of 60 V can be achieved with hafnium dioxide with a typical gap/dielectric thickness of 150 nm [32]. This approach would enable fabrication of a high voltage capacitor in the CMUT layer for compact ultrasound analog front end design in imaging applications. Considering the fact that 64 channel 1-D ICE ASIC occupies 2.6×11 mm^2 [33], this proposed pulser and Tx/Rx switch can fit in ICE application.

IV. CONCLUSION

An integrated supply-inverting HV pulser with Tx/Rx switch is presented in a 0.18-μm 60 V HV-CMOS process to interface with CMUTs in ultrasound systems. The presented circuit overcomes fabrication process limitation by adopting HV protection and bootstrap techniques. The supply-inverted pulser generates 79.6 V of peak-to-peak voltage swing using 45 V of positive supply with 8 pF of equivalent CMUT loading and 30 pF of external capacitance. A bipolar pulse was successfully applied to a CMUT array element and optimized for maximum acoustic pressure. The output followed predictions by a large signal CMUT model, paving the way for large signal simulation-based CMUT-pulser optimization. The proposed Tx/Rx switch effectively blocks the HV swing of the supply-inverted pulser without degrading the performance of the proposed pulser. While the prototype pulser and Tx/Rx switch measurements were conducted with an off-chip capacitor, the technology exists to allow this capacitor to be integrated with the CMUT, using high-K dielectric layers, during CMUT fabrication. On-going research involves co-optimization of the pulser and CMUT arrays using CMUT-on-CMOS technology for compact catheter-based ultrasound imaging systems.

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