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Extreme environment interconnects and packaging for power electronics

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Alberto Campos-Zatarain¹ ⊠, Jack Hinton², Maria Mirgkizoudi², Jing Li², Russell Harris², Robert W. Kay², David Flynn¹

¹Heriot Watt University, Smart Systems Group, Mountbatten Building, Edinburgh, EH14 4AS, Scotland ²Future Manufacturing Processes Research Group, School of Mechanical Engineering, University of Leeds, LS2 9JT, Leeds, UK © E-mail: d.flynn@hw.ac.uk

Abstract: This paper presents the combination of an innovative assembly and packaging process utilising solid liquid inter diffusion (SLID) Cu-Sn interconnects within bespoke ceramic substrates that have been produced using additive manufacturing (AM). The resultant process chain supports the integration and packaging of power electronics for harsh environment applications. Here, the authors explore how the bond strength and composition of Cu-Sn SLID interconnects vary during exposure to thermal-mechanical load profiles. Samples of Cu-Sn are exposed to thermal loading up to 300°C and integrated mechanical loading via high random frequency vibrations (1 and 2000 Hz). In parallel, micro-extrusion printing methods in which high-viscosity ceramic pastes are dispensed through cylindrical fine nozzles (2–250 µm) using CNC-controlled motion has enabled complex 3D geometries to be fabricated. Additional secondary conductor deposition after firing the ceramic substrate enables the electronic circuitry to be generated without dedicated tooling, masks, or templates. This work presents the first fully 3D-printed ceramic-based electronic substrates. To demonstrate the applications of this printing method, a 555 timer circuit with flashing LED has been printed and the components surface mount assembled. The resultant ceramic substrates are dense, mechanically robust, and the reflowed circuit functions exactly as intended.

1 Introduction

Across a myriad of industrial sectors, ranging from aviation, space, subsea, and energy, high value assets are deployed in harsh environments. These environments are typically defined by challenging high values of temperature, pressure, radiation, vibration, and chemically corrosive conditions. The ability to monitor these assets is impeded by several issues related to the thermal limits of materials as aggressive ambient conditions may produce sensor drift and failure, power management, and communication problems. In such applications, electronics are often exposed to temperatures above 200°C, which exceeds the 150°C limit of traditional Si devices if used without extra cooling mechanisms. However, the trends across these sectors indicate a rapidly growing demand for more sensing and electronics within harsh environments [1].

A suitable electronic packaging material for harsh environments are ceramics, engineering ceramics are broadly defined as inorganic, non-metallic materials [2]. Ceramics exhibit a range of desirable material characteristics including high hardness, excellent thermal, and electrical insulation, high resistance to wear, erosion, and corrosion [3]. However, these characteristics present a number of challenges during subsequent formative and manufacturing processes. Conventional methods of manufacture often involve multiple formative and finishing processes that are segregated by a profiled thermal cycle. The hard and brittle nature of ceramic materials results in bulk ceramic being unsuitable for formative and large-scale material removal processes. Therefore, ceramic powder with a narrow particle-size distribution is dispersed within an organic binder and additional additives to improve processability and component performance. The subsequent matrix exhibits suitable fluidity and characteristics to undergo formative processing such as injection moulding [4], extrusion [5], and machining [6, 7]; yielding a near-net-shape green-state ceramic part. Subsequent thermal processing decomposes the organic elements and induces sintering of the remaining inorganic elements.

The thermal processes cause an inherent degree of shrinkage between the green and sintered components, typically 16-18% [8,

9]. Additional finishing procedures such as grinding, lapping, and polishing can be used to improve the geometric tolerances and appearance of the component [10]. However, reliance on component-specific templates and tooling place significant limitation on the flexibility and responsiveness of the manufacturing process. Moreover, tooling-based production methods require volume production to be economically viable, while placing restrictive design constraints on the components that can be manufactured.

Digital-driven manufacturing approaches such as additive manufacturing (AM) is an emerging field of manufacturing approaches that seek to mitigate the short-comings associated with traditional manufacturing approaches. AM produces components directly from digital data in a layer-wise manner, mitigating the need for component-specific templates and tooling [11]. AM techniques originally developed for processing polymers and waxes have been adapted to handle materials such as engineering ceramics. Typically, this involves using conventional materials as a binding medium that is subsequently removed during thermal processing. Despite the relative merits of AM processes capable of processing ceramic materials, the inherent limitations of AM are compounded by the additional processing stages and associated shrinkage, resolution, density, material selection, and compatibility. Hybrid manufacturing is an emerging class of digitally driven manufacturing approaches in which multiple manufacturing approaches are amalgamated into a single, integrated system. We present our preliminary hybrid manufacture results within this paper.

In terms of wideband gap semiconductor materials, SiC is the most mature technology as the fabrication of 300°C integrated circuits and 400°C transistors have been reported already [12, 13]. To take advantage of the thermal properties of such wide band gap materials, the interconnects must also tolerate high temperatures and provide high fatigue resistance. Due to these prerequisites soft solders, thermoplastics and epoxies cannot be considered for die mount due to their low melting temperatures. There are a number of alternative options for interconnects for high temperature applications, including Au thermo-compression bonding, silver





Fig. 1 Thermal-mechanical characterisation system



Fig. 2 Typical random vibration test curve for equipment within a fixedwing aircraft

nanoparticle pastes, Au thick film pastes, and solid liquid inter diffusion (SLID) bonding.

SLID is an interconnection and bonding technique which is based on the rapid formation of an intermetallic compound (IMC) between a high melting point metal and a low melting point metal at a temperature above the melting point of the later. The advantage of the resulting IMC is that it will have a much higher melting temperature than the processing temperature, therefore allowing subsequent manufacturing steps without the need of decreasing processing temperatures [14]. SLID offers several advantages over the other interconnection systems, e.g. it is faster than thermocompression bonding [15], joints show higher shear strength than those created using silver nanoparticles paste [16] and it is less complex with a lower processing temperature than Au thick film materials [17, 18]. Examples of SLID bonding are Ag-In, Ag-Sn, Au-In, Au-Sn, and Cu-Sn systems.

During their lifetime, interconnects used in the aerospace and oil & gas industries are typically exposed concurrently to different loadings such as vibration and thermal shock. However, the contribution of vibration damage to the overall fatigue life of interconnect has not been investigated in any detail previously. Vibration is normally taken as a loading case that only causes elastic material response [19].

In this work, we integrate the advancements from our seminal studies into high temperature interconnects, [20], test vehicles bonded using the Cu-Sn SLID system. In parallel, we also report how micro-extrusion printing methods in which high-viscosity ceramic pastes are dispensed through cylindrical fine nozzles (2–250 μ m) using CNC-controlled motion has enabled complex 3D geometries to be fabricated for high temperature electronic packaging applications. Additional secondary conductor deposition after firing the ceramic substrate enables the electronic circuitry to be generated without dedicated tooling, masks, or templates. This work presents the first fully 3D-printed ceramic-based electronic substrates.

The following section outlines the fabrication process of the demonstrator interconnect devices, test procedure, and profile, and summary of the characterisation method. Section 3 presents the results and discussion relating to the Cu-Sn interconnects, Section 4 outlines the hybrid AM process and finally Section 5 presents the primary conclusions of this research.

2 Methodology for Cu-Sn interconnect characterisation

2.1 Exemplar bond preparation

SLID bonds consisting of Cu-Sn were manufactured by electrodeposition of Cu and Sn on oxidised Si wafers with a nanometer Au seed layer. The initial seed layer was fabricated from a 60 nm TiW adhesion layer, followed by the deposition of a 800 nm Au film which was sputtered onto the TiW layer. Photoligthography using a AZ4562 photoresist was used to create the bond patterns for the Cu and Sn electro-deposition. Ar/O₂ (ratio 3:1) plasma treatment was performed prior to each electro-deposition step to ensure a clean seed layer surface. A 433 nm of Cu and 860 nm was deposited on each wafer using pulse-reverse electroplating. The bias/reverse current density was set to10 mA/cm², with a bias/ reverse pulse of 400 ms/20 ms for both material types.

The dimension of $1.0 \text{ mm} \times 0.8 \text{ mm}$ was patterned onto each sample of silicon wafer. In the next step, wafers were then bonded using a two-step temperature profile, which involved a rapid heat cycle at a rate of 7°C/min and brought into contact at 150°C, initiating the diffusion process between Cu and Sn. This process limits the amount of Sn left in the bond line when reaching the melting temperature of Sn at 231.9°C, thus reducing the amount of Sn material loss. After which the silicon test pieces are heated at a rate of 3°C/min until reaching 260°C. Following this step, they are soaked for a minimum of 10 min, allowing the bond line to be converted to Cu/Cu₃Sn/Cu IMC. While maintaining a temperature of 150°C, the wafers were bonded using a bonding pressure of 20 MPa. For more information about the fabrication process refer to [20, 21].

2.2 Characterisation system

The thermal-mechanical loading system was constructed from two primary sub-systems: (i) a LDS-V650 electrodynamic shaker and (ii) a thermal hot plate. A vibration control and data acquisition system was integrated into the system so that we could design and implement the vibration tests. The thermal plate was attached to the shaker head. The thermal plate was energised and controlled by a temperature controller. Fig. 1 shows the final thermal-mechanical characterisation system.

2.3 Thermal-mechanical test profiles

For the thermal-mechanical testing, six sets of Cu-Sn bonded samples were exposed to the standard random vibration test profile, shown in Fig. 2 [22], along with temperature loads at 25, 100, 200, and 300°C. The thermal-mechanical tests were founded on the RTCA/DO-160E Environmental Conditions and Test Procedures for Airborne Equipment standard. Experiments were performed in three orthogonal axes for 60 min per-axis (total of 180 min per test). The frequency of the tests ranged from 10 to 2000 Hz and the acceleration power spectral density (APSD) from 0.02 to 0.08 G^2 /Hz. The APSD levels that correspond to each test curve frequency break point can be found in Table 1 [22].

Analysis method: Shear testing was used to characterise the mechanical strength of the bond pads after thermal-mechanical loading. To enable a calculation of the effective shear strength, the bonded area must be known. Samples were also sectioned so that they could be analysed by optical microscopy and scanning electron microscopy (SEM).

2.4 Shear characterisation

The die shear tests were performed using a Dage Series 4000 Bondtester with a 100 kg load cartridge. The shear tool height was

Table 1 Acceleration power spectral density levels

Test levels at test curve frequency break points						
frequency, Hz	10	28	40	250	500	2000
APSD, G ² /Hz	0.02	0.02	0.04	0.04	0.08	0.02



Fig. 3 Measured shear strength for sets of samples exposed to integrated thermal-mechanical load profiles



Fig. 4 Recorded shear strength values for samples exposed only to thermal loading

set to 560 nm above the surface of the substrate and shear speed of 700 nm/s. Die shear characterisation was implemented on four of the six bonded exemplars from each set with the remaining two samples used for cross-sectional analysis (c.s.a).

2.5 Cross-sectional analysis

On completion of testing, two samples from each of the sets were diced using a 3000-nm-thick fully sintered diamond blade which rotates at 13,000 RPM. The c.s.a was initially conducted without polishing, using a Leica DM6000 M microscope with an N Plan L 100X/0.75 BD objective.

3 Results and discussion

3.1 Shear strength results

Fig. 3 displays the average die shear strength for sets of four bonded test pieces after exposure to the thermal-mechanical loading outlined in Section 2.3 and Fig. 4 shows results from samples only exposed thermal loading without the vibration/ mechanical shock.

As shown within Figs. 3 and 4, the bonds that were exposed to thermal-mechanical effects exhibit an increase in die shear force, with the 300°C samples showing an increase of 40 MPa. All of the sample sets exhibit an increase in die shear strength beyond 100°C, at 300°C, there is a compositional transition in the form of an



Fig. 5 C.S.A of an interconnect exposed to vibration @21°C



Fig. 6 C.S.A of an interconnect with vibration loading @100°C



Fig. 7 C.S.A of an interconnect with vibration loading @200°C

increasing alloy presence as a product of the Cu layers becoming incorporated within the CuSn thin film.

3.2 Microstructural analysis

On completion of c.s.a, the images within Figs. 5–8 show the cross-section of samples exposed to thermal-mechanical testing at 21, 100, 200, and 300°C, respectively.

The optical microscopy images indicate that there is a gradual increase in the alloy composition within the interconnect structure. This appears to be the reason behind the increasing shear strength of these particular bonded samples.



Fig. 8 C.S.A of an interconnect with vibration loading @300°C



Bespoke 5-axis micro-extrusion system



Multilayer 3D printing process 3D fe

3D formed green part

Fig. 9 5 axis micro-extrusion system, image of the 3D printing process

4 Additive manufacturing of ceramic packaging

A 5-axis table is used to drive the dispensing head with motion accuracy $\pm 25 \,\mu$ m, shown in Fig. 9. The dispensing head equipped with a piezoelectric actuator is used for printing of a small particle size distribution alumina-based paste supplied by Morgan Advanced Materials which exhibited the required viscoelastic characteristics to enable printing successfully down through 150 μ m nozzles. The printing process begins by extruding a perimeter defining the layer features. The layer is then in-filled using a rectilinear infill pattern. The process is then repeated layer-by-layer to build up the substrate. In this case, four layers have been printed. The green part is then fired at 1600°C and shrinkages around 15% from the process.

Cross-sectioning of the substrate reveals a high density fired part with the printed layers not visible, shown in Fig. 10. However, polishing of the cross-sectioned samples needs to be improved as grains have been cleaved from the sample surface. Also, elimination of air entrapment in the paste prior to printing is required.

The Ag filled LTCC paste was selectively deposited onto the fired ceramic substrate. To test the feasibility of this process, a surface mount 555 timer circuit with flashing LED, timer chip, and discrete components was designed. The circuit was deposited using a 200 μ m nozzle. After printing, the substrate was fired again using a profile of 3°C/min to 100°C, 2°C/min to 450°C, 10°C/min to 865°C and hold for 20 min. The final line width after firing was ~700 μ m. Using a smaller nozzle diameter in addition to



Fig. 10 Cross-section of the ceramic microstructure



Fig. 11 Functioning 555 timer circuit produced using digitally driven additive manufacturing

adjustments to the rheological properties of the paste material and a reduction of particle size could enable a smaller nozzle diameter and resulting finer track widths.

The fired conductor lines exhibited a strong adhesion to the ceramic substrate and a low resistance similar to conventional LTCC conductive tracks. The ceramic substrate was processed using a conventional surface mount assembly process of solder paste deposition, pick and place of the individual components followed by a reflow process in a convection oven. The 555 timer circuit consists of three capacitors, one LED, four resistors, one transistor, and one 555 timer, shown in Fig. 11. The solder paste was dispensed rather than using a stencil template in order to prove this whole process could be digitally driven thereby enabling mass-customised production of parts and also rapid iterative product development.

The first board assembled and reflowed worked exactly as intended thereby proving the feasibility of this approach. This work demonstrates the world's first fully 3D-printed ceramic electronic substrate completely compatible with conventional surface mount packaging.

5 Conclusions

Within this paper, we have demonstrated how hybrid manufacturing can produce harsh environment electronic packaging. Predominant methods of manufacturing ceramic components use template-driven methods, which hampers responsiveness and impose significant design constraints. This has driven significant interest towards digitally driven manufacturing approaches, primarily, AM. AM has demonstrated the rapid production of bespoke and highly complex geometries and designs direct from digital data without the need for component-specific tooling. Yet, when used in isolation, these techniques are restricted by uncontrollable porosity, high shrinkages during firing plus a lack of process-compatible materials. This paper presents the research and development of a new hybrid manufacturing process chain for the agile production of engineering grade ceramics components. The combination of high-viscosity ceramic paste extrusion, sacrificial support deposition and subtractive micromachining has yielded complex monolithic ceramic components demonstrating feature sizes of 100 µm, part densities of ~99.7%, surface roughness down to ~1 µm Ra, and 3-point bend strength of 218 MPa. Integrating wide band gap semiconductor materials namely SiC within the ceramic packaging also necessities interconnects that can withstand thermal mechanical loads. Within this research, we have fabricated, characterised, and analysed CuSn interconnects for harsh environment applications. The suitability of this interconnect technology has been validated through the seminal testing with a custom shake & bake system, with 90 MPa shear strength recorded at 300°C under thermal/mechanical loading. The compositional changes with temperature appear to influence the die shear strength of the samples. Interestingly, the influence of the vibrational forces has further enhanced this property.

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7 References

- [1] Senesky, D. G., Jamshidi, B., Cheng, K. B., et al.: 'Harsh environment silicon carbide sensors for health and performance monitoring of aerospace systems:
- a review', *IEEE Sens. J.*, 2009, **9**, pp. 1472–1478 Warlimont, H.: '*Ceramics BT springer handbook of condensed matter and materials data*', in Martienssen, W., Warlimont, H., (Eds.) (Springer Berlin [2] Heidelberg, Berlin, Heidelberg, 2005), pp. 431-476
- [3] Wachtman, J. B., Cannon, W. R., Matthewson, M. J.: 'Mechanical properties of ceramics' (John Wiley & Sons, Hoboken, 2009)
- Edirisinghe, M. J., Evans, J. R. G.: 'Fabrication of engineering ceramics by [4] injection moulding. II. Techniques', Int. J. high Technol. Ceram., 1986, 2, (4), pp. 249–278
- Ribeiro, M. J., Ferreira, J. M., Labrincha, J. A.: 'Plastic behaviour of different [5] ceramic pastes processed by extrusion', Ceram. Int., 2005, 31, (4), pp. 515-519
- [6] Tuersley, I. P., Jawaid, A., Pashby, I. R.: 'Various methods of machining advanced ceramic materials', J. Mater. Process. Technol., 1994, 42, (4), pp. 377-390

- [7] Belous, K. P.: 'Machining of ceramic materials', Chem. Pet. Eng., 1972, 8, (5), pp. 447-449
- Ozer, I. O., Suvaci, E., Karademir, B., et al.: 'Anisotropic sintering shrinkage in alumina ceramics containing oriented platelets', J. Am. Ceram. Soc., 2006, [8] 89, (6), pp. 1972-1976
- Shui, A., Zeng, L., Uematsu, K.: 'Relationship between sintering shrinkage [9] anisotropy and particle orientation for alumina powder compacts', Scr. Mater., 2006, 55, (9), pp. 831-834
- Doi, T., Uhlmann, E., Marinescu, I. D.: 'Handbook of ceramics grinding and [10] polishing' (William Andrew, Oxford, 2015)
- Mueller, B.: 'Additive manufacturing technologies-rapid prototyping to direct [11] digital manufacturing', Assem Autom., 2012, **32**, (2), pp. 378–399 Clark, D. T., Ramsay, E. P., Murphy, A. E., et al.: 'High temperature silicon
- [12] carbide CMOS integrated circuits', in The 8th European Conf. on Silicon Carbide and Related Materials (ECSCRM 2010), Oslo, Norway, 2010, pp. 726-729
- Thompson, R. F., Clark, D. T., Murphy, A. E., et al.: 'High temperature silicon carbide CMOS integrated circuits'. IMAPS High Temperature [13] Electronics Network (HiTEN 2011), Oxford, UK, 2011, pp. 115-119
- Tollefsen, T. A., Larsson, A., Løvvik, O. M., et al.: 'High temperature [14]
- [15]
- Tolletsen, T. A., Larsson, A., Løvvik, O. M., et al.: "High temperature interconnect and die attach technology: Au–Sn SLID bonding", *IEEE Trans. Compon. Packag, Manuf. Technol.*, 2013, **3**, pp. 904–914
 Tolletsen, T. A., Larsson, A., Løvvik, O. M., et al.: 'Au-Sn SLID bonding— properties and possibilities', *Metall. Mater. Trans. B*, 2012, **43**, pp. 397–405
 Masson, A., Buttay, C., Morel, H., et al.: 'High-temperature die-attaches for SiC power devices'. 14th European Conf. on Power Electronics and Amplications (IEEE FDE 2011). Disminichem LW, 2011, en p. 101 [16] Applications (IEEE EPE 2011), Birmingham, UK, 2011, pp. 1-10
- [17] Salmon, J. S., Johnson, R. W., Palmer, M.: 'Thick film hybrid packaging techniques for 500°C operation'. 1998 Fourth Int. High Temperature Electronics Conf. (HiTEC), Albuquerque, New Mexico, USA, 1998, pp. 103-108
- [18] Chen, L. Y., Hunter, G. W., Neudeck, P. G.: 'Silicon carbide die attach scheme for 500°C operation'. MRS 2000 Spring Meeting Proc.-Wide-Bandgap Electronic Devices (Symp. T), San Francisco, California USA, 2000
- [19] Basaran, C., Cartwright, A., Zhao, Y.: 'Experimental damage mechanics of microelectronics solder joints under concurrent vibration and thermal loading', Int. J. Damage Mech., 2001, 10, pp. 153–170
- Campos-Zatarain, A., Flynn, D., Aasmundtveit, [20] Κ E et al· 'Characterization of Cu-Sn SLID interconnects for harsh environment applications'. IEEE Symp. on Design, Test, Integration and Packaging of MEMS/MOEMS, Cannes, France, 2014, pp. 1–8, DOI: 10.1109/ DTIP 2014 7056665
- [21] Luu, T. T., Duan, A., Aasmundtveit, K. E., et al.: 'Optimized Cu-Sn waferlevel bonding using intermetallic phase characterization', J. Electron. Mater., 2013, 42, pp. 3582-3592
- [22] I. RTCA: 'RTCA aviation standard DO-160E, 'Environmental conditions and test procedures for airborne equipment'. ed. Washington, 2004