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Impact of Poly-Crystalline Diamond within Power Semiconductor Device Modules in a Converter

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***Abstract*—This paper presents the finding of thermal characterization of polycrystalline diamond for power semiconductor device modules in a converter. Comparisons of measured thermal performance of two diamond demonstrators, consisting of metalized diamond tiles attached to aluminum and copper forced air cooled heat sinks; show that power dissipation can be increased from 278W to 535W when compared to commercial products operating at a case temperature of 100°C and a maximum junction temperature of 175°C. Detailed converter simulations of a two level three-phase inverter driving a 15kW permanent magnet machine shows that using diamond can increase active power density from 13kW/kg to 17kW/kg at a coolant temperature of 100°C and a flowrate of 6 liters per minute.**

Keywords—Power electronic converter sizing, Diamond heat spreaders, Power Density, Power electronic systems.

I. INTRODUCTION

There is a significant demand for power dense power electronic systems driven by the necessity for increased power rating within a given footprint. Fig. 1 shows a typical cross-section of a power semiconductor module. For a given semiconductor device solution, the realizable power rating is limited predominantly by the ability to dissipate the power loss generated by the device whilst maintaining the junction temperature within its maximum operating temperature limit. Fig. 2 shows the thermal path from the semiconductor die to ambient. The power loss which can be tolerated is itself inversely proportional to the thermal resistance from the junction to the surrounding ambient. Reliability of the semiconductor devices are significantly affected by maximum junction temperature and temperature swing, imposing maximum limits with respect to device type and packaging technology. Therefore, one of the key options to increase converter power density is to reduce the junction-to-case thermal resistance [1][2][3] by using materials with combined high dielectric strength and thermal conductivity.

Power semiconductor device modules generally use alumina (Al_2O_3) or aluminum nitride (AlN) for the isolation layer between the top and bottom metallization layers. Generally, Al_2O_3 is used for low cost products whereas AlN is targeted towards higher performance applications due to its greater thermal conductivity, higher cost and better matched coefficient of thermal expansion to silicon and silicon carbide power devices. Fig. 3 shows a disaggregation of the overall thermal resistance from the silicon die to case considering an AlN substrate attached to a copper heat spreader. As shown, the heat spreader and substrate contribute substantially to the overall thermal resistance, therefore by using a tile material with combined high thermal conductivity and high critical electric field strength, such as diamond, significant reductions in the overall thermal resistance can be achieved, resulting in a subsequent increase power density of the power semiconductor module which can be exploited by the power electronics converter.

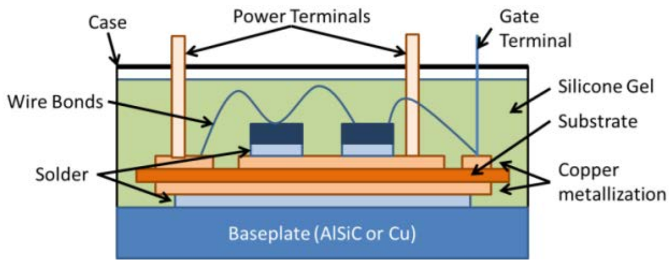

Fig. 1: Cross-section of a typical power semiconductor device module

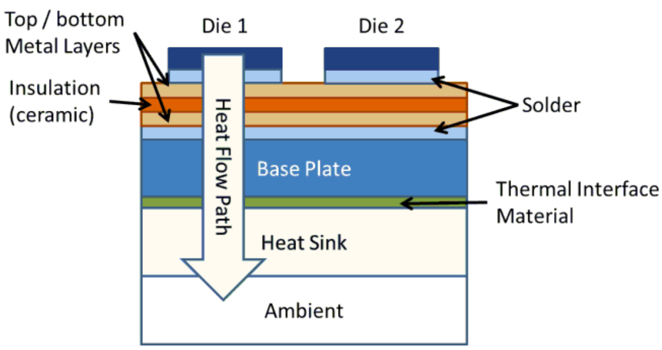

Fig. 2: Thermal path from die to ambient

Diamond has directed much attention as an alternative material for active electrical devices [5], packaging material [7] or heatsinks [8]. Due to the high substrate cost, diamond coated layers are normally preferred where a substrate material, AlN for

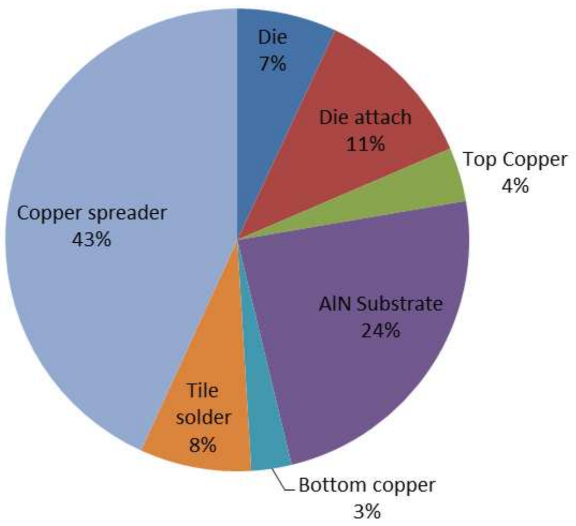

Fig. 3: Disaggregation of thermal resistance contributions for a silicon die attached to an AlN substrate with a copper heat spreader

example, is coated with a thin diamond film [9]. These have shown improved thermal performance of the substrate medium; however, due to the binding materials, these do not achieve the full potential that diamond can offer. Simulation and small scale electrical results have been previously reported for dies attached to Chemical Vapor Deposited (CVD) and polycrystalline diamond [11][12][13], demonstrating improvements diamond can offer in terms of thermal resistance by means of small scale electrical measurements or numerical modelling. In this paper the performance of a diamond demonstrator consisting of silicon and silicon carbide power devices attached to a metallized polycrystalline diamond substrate is investigated. After tile assembly, these are subsequently attached to a copper or aluminum air cooled heat-sink. These devices are thermally characterized up to a loading of 200W (~200W/cm^2); typical conditions the devices would exhibit during power rating of a typical module [16]. Thermal resistance measurements are used to predict performance benefits of a module consisting of a diamond tiles compared to commercially available power semiconductor modules using the same IGBT die technology.

II. Diamond Demonstrator

For the diamond demonstrator, two heat sink materials were considered, viz. aluminum and copper. These were forced air cooled heat sinks combining fin and impingement cooling techniques. To measure tile performance, a simple chopper circuit was implemented on the top metallization layer. Fig. 4 shows the top copper layout and power circuit used for the demonstrator. The layout was design to accept 1 x 100A 1200V IGBT [14] and 2 x 1200V 50A Schottky diodes [15] to give a maximum current rating of approximately of 100A. An exclusion zone of 1mm was incorporated around each die and bond areas and a 2mm tracking distance between high and low voltage lines was used. The bond landing sites for the gate and emitter sense are sufficient to accept 500µm wire whereas the anode/cathode sites were sized to obtain current levels greater than 200A.

To assess the performance of the demonstrators, a Temptronic Thermostream, TP04310, was used as an air supply, and the devices were subjected to a maximum DC current loading of 80A to self-heat the samples to a junction temperature of approximately 150°C. To determine the case temperature, average temperature readings were inferred from four thermocouples embedded within the heat sink, surrounding the diamond tile. Two passive probes were used to determine the anode and cathode voltage and deduce forward voltage drop of the Device Under Test (DUT). Current measurements were performed with Agilent 30A and 150A DC current probes (N2783A/N2781A). Fig. 6 shows the thermal test rig and a diamond demonstrator under test. After the demonstrator has thermally stabilized, the die is used as an indirect temperature sensor by reference the measured forward voltage drop and DC current level to calibration curves, as shown in Fig. 7 and Fig. 8. From the junction-to-case temperature and the power levels the thermal resistance of the sample can be determined.

Measured junction and case temperature with respect to input power of the IGBT die is shown in Fig. 9. As shown, as the applied DC power increases the junction and case temperatures increase as a result of the thermal flux. Fig. 10 shows the measured junction-to-case thermal resistance calculated from this measurement data. For this DUT, at a die

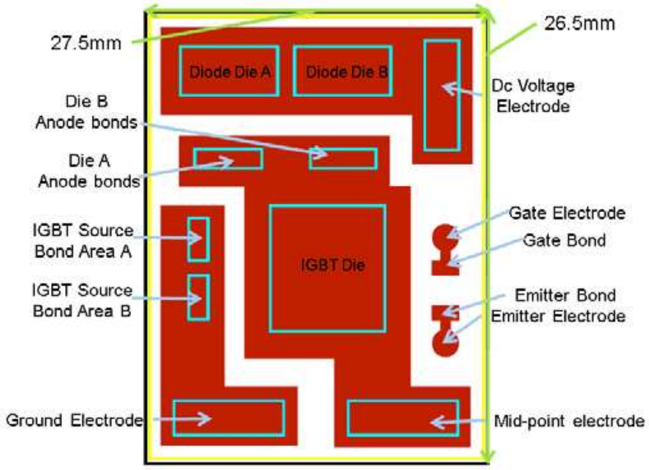

Fig. 4: Top copper layout of the demonstrator

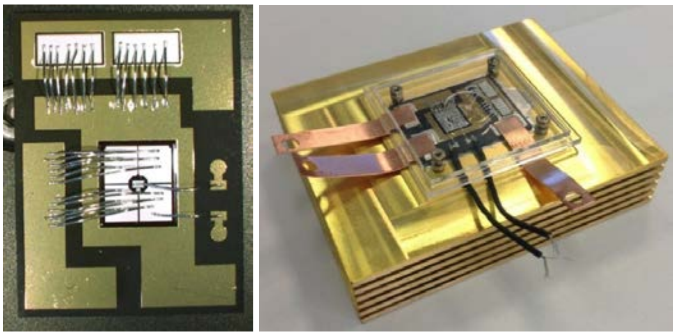

Fig. 5: Diamond tile post wire bonded and attached to the heatsink.

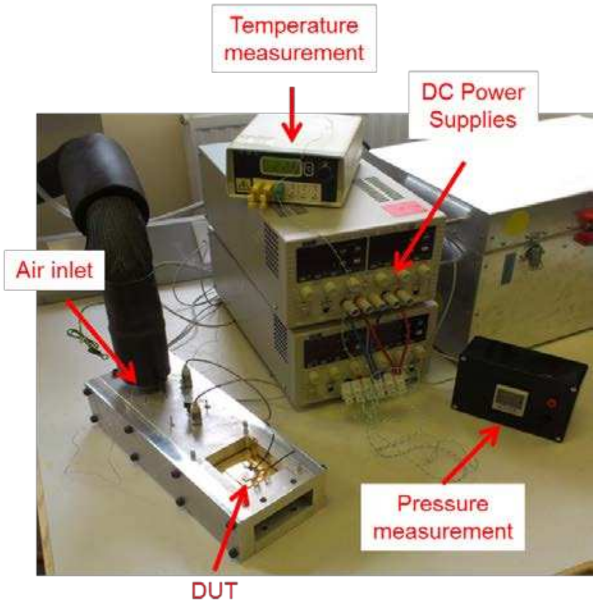

Fig. 6. Diamond demonstrator and device under test

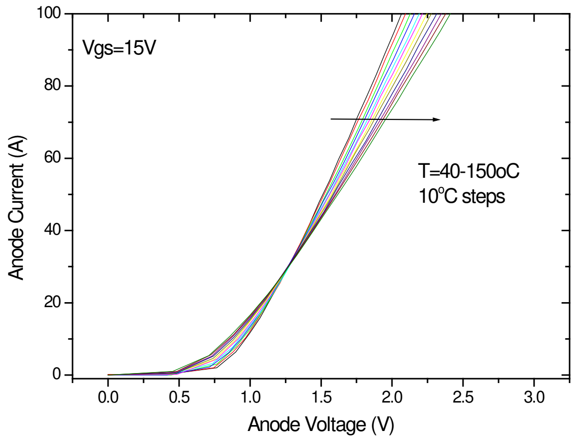

Fig. 7: Measured current-voltage characteristics of IGBT die at various temperature operating points (V_{gs} = 15V)

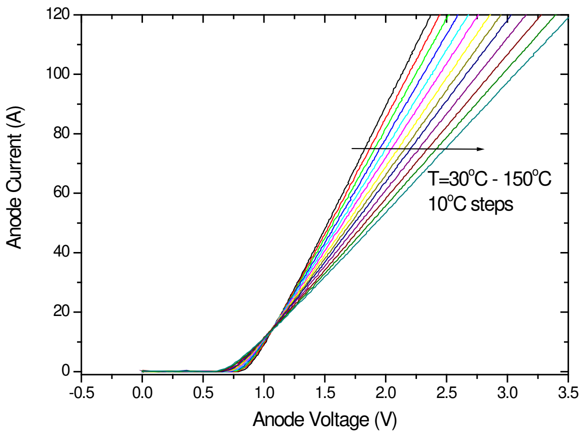

Fig. 8: Measured diode current-voltage characteristic at various temperature operating points

thermal loading of 150W, a junction-to-case thermal resistance of 0.19K/W is obtained. The non-linear relationship between power and thermal resistance is attributed to the thermal spreading of the DUT with applied power. Measured thermal resistance of the silicon carbide Schottky diodes and both copper and aluminum heatsinks are shown in Table 1. As shown, the devices attached to the copper heat sink obtain lower thermal resistance, due to its higher thermal conductivity compared to aluminum. Fig. 11 compares the IGBT junction-to-case thermal resistance of the diamond demonstrators to commercial products using the same die [16][17][18]. For this comparison, the diode technologies have been disregarded due to difference in current rating and device type. As shown, the magnitude of measured thermal resistance of the diamond demonstrators is significantly lower than that of the commercial products. This reduction in thermal resistance can effectively increase the device power rating from 278W to 395W/535W for the aluminum/copper mounted demonstrators respectively, assuming a maximum junction temperature of 175°C and a case temperature of 100°C.

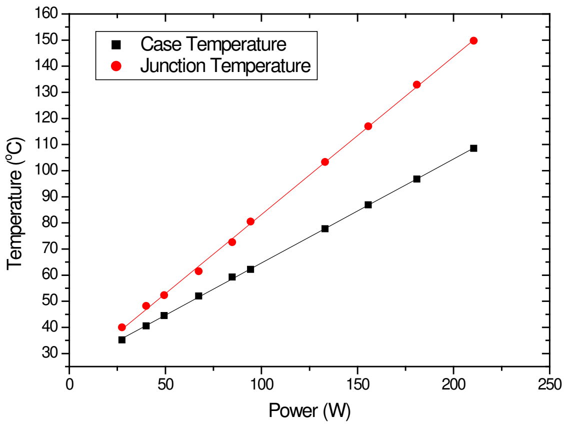

Fig. 9. Measured junction and case temperatures of the IGBT for the diamond tile attached to the Aluminum heat-sink with respect to temperature

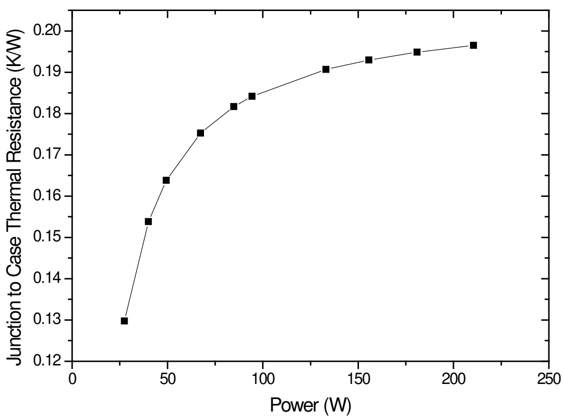

Fig. 10. Calculated junction to case thermal resistance of the IGBT for the diamond tile attached to the Aluminum heat-sink with respect to temperature

Table 1:Measured thermal resistance for IGBT's and diodes attached to the diamond tiles at a thermal power loading of 150W

Heat-Sink	Thermal resistance taken at 150W thermal loading	
	IGBT	SiC Schottky Diode
Aluminum	0.19 K/W	0.13 K/W
Copper	0.14 K/W	0.091 K/W

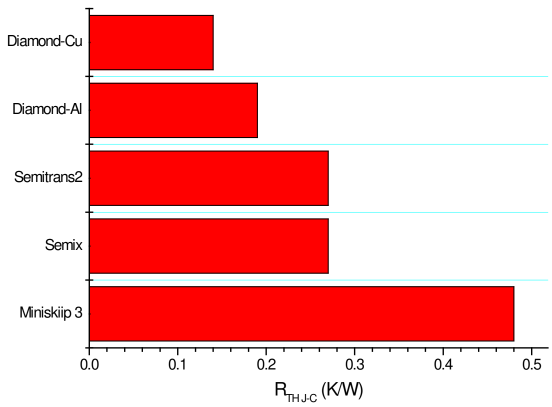

Fig. 11:Thermal resistance comparison on the diamond demonstrator compared to commercial technologies using the same IGBT die

III. Power Converter Model

To measure the impact a diamond tile has on the size of a power electronics converter, a power electronics sizing tool was developed to study the impact of diamond on a three-phase inverter driving a 15kW machine, as shown in Fig. 12. The size and weight of the DC-link capacitor and heatsink are calculated to drive the machine in a motoring condition at 20krpm, sourced from a 270V DC network. The permanent magnet motor is a four pole machine with a back emf coefficient of 21mV/rad/s, phase self-inductance of 98.7µH and resistance of 30mΩ. Due to the power factor of the converter operating at this specific design point, the converter has to be rated at ~25kW to supply the 15kW load.

To calculate the power losses in the semiconductor devices, a single phase equivalent was considered assuming that all phase currents and voltages are equal, Fig. 13. Using a space vector modulation strategy with a modulation index of 1, the maximum voltage applied from a single output phase is limited to 110V, as given by (1).

$$V_{i-N} = \frac{V_{DC}}{\sqrt{2}\sqrt{3}} \tag{1}$$

For the machine and operating conditions, the maximum voltage applied across the phase windings (V_p) would be 101V (2) giving a maximum output phase current of 244A (4).

$$V_p = \sqrt{{V_{i-N}}^2 - {V_e}^2} \tag{2}$$

$$V_{i-N} = \frac{V_{DC}}{\sqrt{2}\sqrt{3}} \tag{3}$$

$$I_p = \frac{V_p}{X_p} \tag{4}$$

Therefore at this speed the maximum output from this machine is 16kW, for this analysis this was reduced to 15kW, i.e. at a point where the converter modulation index is close to 1.

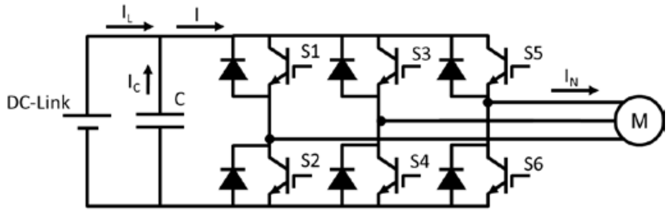

Fig. 12: Circuit under study

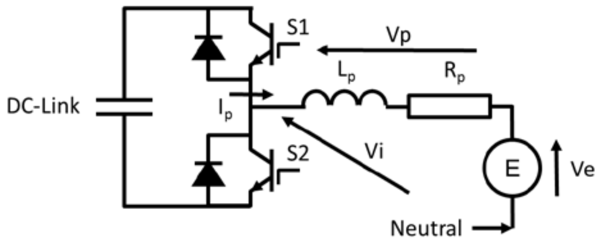

Fig. 13: Single phase representation of the converter

In order to size the power converter, the losses associated with the semiconductor devices need to be calculated with respect to the operating conditions; associated from when the device is operating in the on-state and during switching transients. The power factor of the converter can be obtained by (5), from which the average and rms current levels seen from the IGBTs (Q) and anti-parallel diodes (D) of the individual phase legs can be obtained (6-7), where m_i is the modulation index [19].

$$PF = \cos\left(tan\left(\frac{V_p}{V_e}\right)^{-1}\right) \tag{5}$$

$$I_{Q\,rms} = I_p\sqrt{\frac{1}{8} + \frac{M_i cos(PF)}{3\pi}}$$
$$I_{D\,rms} = I_p\sqrt{\frac{1}{8} - \frac{M_i cos(PF)}{3\pi}} \tag{6}$$

$$I_{Q\,ave} = I_p\left(\frac{1}{2\pi} + \frac{m_i \cos(PF)}{8}\right)$$
$$I_{D\,ave} = I_p\left(\frac{1}{2\pi} - \frac{m_i \cos(PF)}{8}\right) \quad (7)$$

From (5-7) the on state losses of the IGBT and diodes can be calculated by using (8) where R_{DS} is the effective on-state resistance and V_k is the knee voltage of a linearized current-voltage characteristics. For this analysis, the knee voltage and on-state resistance have been extracted at a maximum junction temperature of 150°C.

$$P_{Q\,ON} = I_{Q\,RMS}{}^2 R_{Q\,DS} + I_{Q\,AVE} V_{k\,Q}$$
$$P_{D\,ON} = I_{D\,RMS}{}^2 R_{D\,DS} + I_{D\,AVE} V_{k\,D} \quad (8)$$

Switching losses of these components are obtained from (9), where F_s is the IGBT switching frequency, E_{on}/E_{off} are the turn on/off losses from the IGBT and E_{rr} the reverse recovery losses from the power diode.

$$P_{sw} = \frac{F_s(E_{on} + E_{off} + E_{rr})}{\pi} \quad (9)$$

The overall semiconductor power losses are the sum of the on-state and switching losses (8 – 9). The semiconductor power losses and their thermal ratings are used as inputs for the heatsink sizing tool.

The heatsink considered in the model is a liquid cooled cold plate using a glycol/water mix of 25% at a temperature of 100°C. From the physical parameters of the coolant and flow rate, the Nasselts number is obtained whether the fluid is in turbulent or laminar flow. From this, the thermal resistance of the equivalent resistive network is solved (10-15) where the total thermal resistance is given by (16) and heat transfer coefficient for the heatsink is obtained [21]. Depending on the footprint of the power module and the required heat sink area, the module/heatsink assembly is sized. For this analysis, the smallest heatsink area is limited to the footprint of the power module.

$$h = \frac{N_u \lambda_{h_2O}}{d_h} \quad (10)$$
$$R_A = \frac{1}{hLc} \quad (11)$$
$$R_a = \frac{1}{hLB_{MI}} \quad (12)$$
$$R_{FIN} = \frac{0.5c}{0.5\left(\frac{b}{N} - B_{MI}\right) L\lambda_{HS}} \quad (13)$$
$$R_{th,d} = \frac{T_{base}}{\frac{1}{N} Lb\lambda_{HS}} \quad (14)$$
$$R_{tha} = R_{FIN} + R_A \quad (15)$$
$$R_{TH,n} = \frac{1}{N}(R_{TH,d}) + \frac{0.5}{V\rho \dot{c}_{p,fluid}} \quad (16)$$

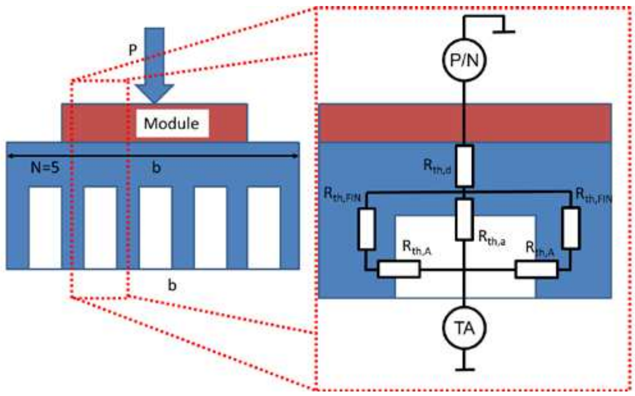

Fig. 14: Equivalent circuit diagram used for heatsink design

Due to absence of DC link voltage quality for the proposed application, the size of the DC-link capacitance can be determined by it associated power losses, internal thermal resistance, hot spot and ambient temperature (17); where T_c, T_a, R_{ESR}, $R_{th\,c\text{-}a}$ and I_C are the hot spot/ambient temperature, series resistance, thermal resistance and capacitors RMS current respectively. For this analysis a 700V 280µH power electronic capacitor used as a unit size which is assumed to be operating in an ambient temperature of 70°C and a maximum hotspot temperature of 85°C [22].

$$T_C = T_a + I_{c,rms}{}^2 R_{ESR} R_{th\,c-a} \quad (17)$$

The capacitor current consists of two current components originating from the fundamental and high switching frequency harmonics. The current due to the fundamental frequency is given by (18) with respect to the modulation index, phase current and power factor of the converter [22].

$$I_{c\,rms} = I_{N,rms}\sqrt{\left[2M_i\left\{\frac{\sqrt{3}}{4\pi} + cos^2\phi\left(\frac{\sqrt{3}}{\pi} - \frac{9}{16}M_i\right)\right\}\right]} \quad (18)$$

The high frequency capacitor current originating from the phase ripple current due to the PWM frequency and load inductance can be expressed as (19) [24], with respect to the position within the space vector reference frame (ϑ) and the product of M_iCos(ϑ).

For: 0°<ϑ<60° and 0<$M_i$cos(ϑ)<1/3

$$I_{pp} = \frac{1}{L_p}(V_{DC} M_i cos(\vartheta) t_o) \quad (19a)$$

For: $1/3 < M_i \cos(\vartheta) < 1/\mathrm{sqrt}(3)$

$$I_{pp} = \frac{2}{L_p}\left(\begin{array}{c} V_{DC} M_i cos(\vartheta) \frac{t_o}{2} + \\ \left(V_{DC} M_i cos(\vartheta) - \frac{V_{DC}}{3}\right) t_2 \end{array} \right) \tag{19b}$$

$0^o < \vartheta < 60^o$

$$I_{pp} = \frac{2}{L_p}\left(\begin{array}{c} V_{DC} M_i cos(\vartheta) \frac{t_o}{2} + \\ \left(V_{DC} M_i cos(\vartheta) + \frac{V_{DC}}{3}\right) t_2 \end{array} \right) \tag{19c}$$

IV. Analysis of Polycrystalline Heat Spreaders

To analyses the impact of polycrystalline diamond, equations (1-19) are implemented into Mathworks Matlab. For this analysis, a 1200V 100A SemiTrans2 [16] module was used as the base line IGBT technology for each phase leg of the converter. The junction to case thermal resistance was modified to represent a diamond tile technology. The influence of PWM frequency upon heatsink weight is shown in Fig. 15. As semiconductor losses increase with frequency, the area of the heatsink increases in order to maintain junction temperatures within their thermal boundaries. Therefore, for a low PWM frequency, the heatsink mass is constant, due to limits imposed by the model to limit heatsink area to the module footprint. As the switching frequency increases, eventually the heatsink area is greater than that of the module footprint and therefore mass increases significantly, as shown in Fig. 15 when switching frequency is increased beyond 5kHz.

Fig. 16 shows the influence of ripple and fundamental capacitor current with respect to switching frequency. The DC-link capacitor is sized on its total current, consisting of the sum of the fundamental and high switching frequency components. At low switching frequencies, the high frequency current component dominates capacitor size due to significant ripple current in the output phase current; whereas for a high frequency capacitor current is dominated by the fundamental current component. For example, at a low switching frequency a DC-link capacitance of five parallel capacitors is required to maintain the hotspot below 85°C. As the switching frequency is increased beyond 9kHz, this is reduced to a single capacitor due to the reduction of ripple current as the capacitor size is governed by the fundamental current component.

When the sizes of heatsink/module assembly and DC-link capacitance are known, the total weight of the active components can be calculated for a given operating condition. Fig. 17 shows the influence of PWM frequency upon gravimetric power density of the converter at a heatsink flowrate of 10 liters per minute. The stepped nature of this figure is due to the capacitor reducing in discrete component size. Due to the influence switching frequency on the size of the heatsink and DC-link capacitor, a maximum power density is achieved when their combined influences are at their minimum. For example, at low switching frequencies power density is limited by the size of the DC-link capacitor as a result of high output ripple currents whereas at high switching frequency heatsink size dominates due to increased power

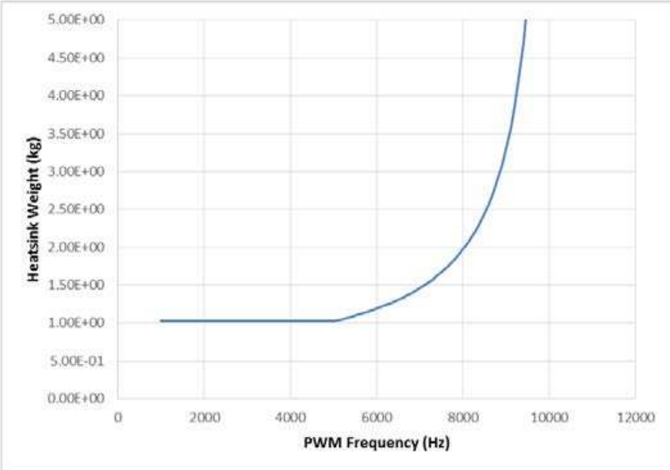

Fig. 15: Influence of PWM Frequency upon Heatsink Weight. (Baseline technology, coolant flow-rate=6LPM, $T_{coolant}$=100°C T_{jmax}=150°C)

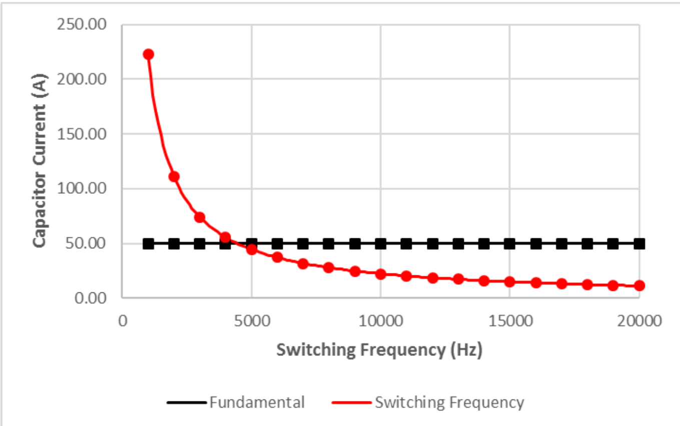

Fig. 16: Influence of PWM frequency and capacitor ripple current (Baseline technology, coolant flow-rate=10LPM, $T_{coolant}$=100°C T_{jmax}=150°C)

losses. Fig. 18 shows the influence of coolant flow rate upon gravimetric power density of the power converter for a benchmark module and module using a diamond tile substrate. As shown, due to the lower junction-to-case thermal resistance, the gravimetric power density saturates at 17kW/kg compared to 13kW/kg for the benchmark module at a coolant flow rate of 6 liters per minute and a maximum junction temperature of 150°C. This is a direct result of the switching frequency reducing the sensitivity of heat sink size with respect to frequency and enabling a smaller combined heatsink and DC-link capacitor size. Due to the relationship of power density and thermal boundaries, Fig. 19 shows the dependency of gravimetric power density with respect to maximum junction temperature. As shown, as the junction-to-case temperature reduces the diamond solution provides improved gravimetric power density as the converter can operate at a higher switching frequency, reducing the size of the DC-link capacitance. However, as the junction temperature increases the power densities eventually over-lap, showing no benefit for the diamond technology. This is due to the higher switching frequency obtained from the diamond component has not resulted in a reduction in DC-link capacitance as it is dominated by fundamental current component.

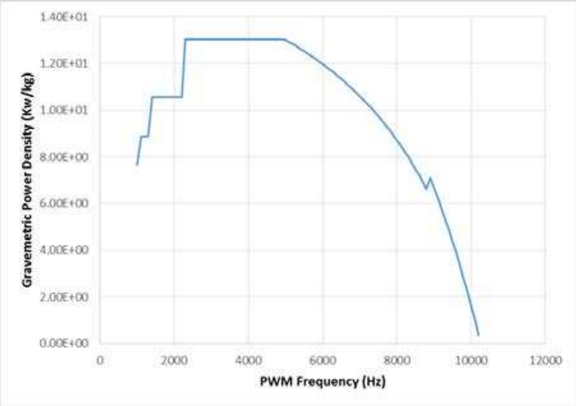

Fig. 17: Influence of PWM frequency upon gravimetric and volumetric power density (Baseline technology, coolant flow-rate=10LPM, $T_{coolant}$=100°C T_{jmax}=150°C)

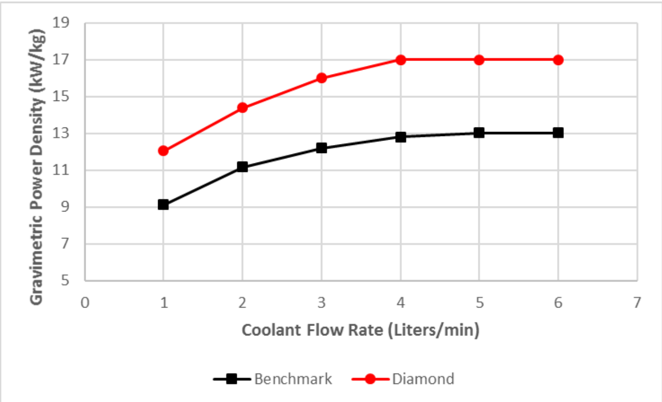

Fig. 18: Comparison of standard modules and diamond spreaders with respect to coolant flowrate ($T_{coolant}$=100°C T_{jmax}=150°C)

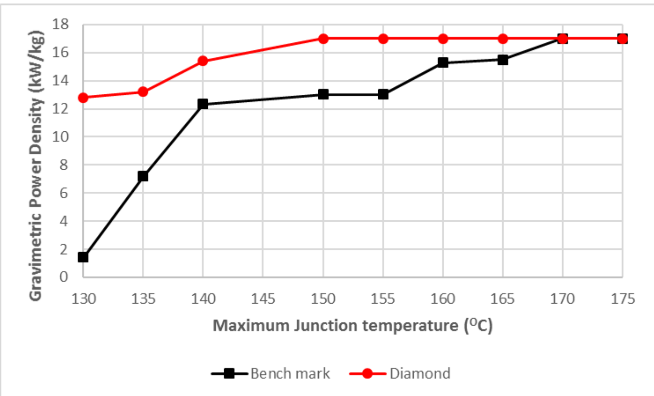

Fig. 19: Gravimetric power density with respect to maximum Junction Temperature (Coolant flow-rate=6 LPM, $T_{coolant}$=100°C)

V. CONCLUSIONS

This paper presents thermal characterization of power semiconductor device attached to metallized polycrystalline diamond tiles. The diamond demonstrator shows that compared to current substrate technologies, for a maximum junction temperature of 175°C and a base plate temperature of 100°C the maximum dissipated power can increase from 278W to 535W. Electro-thermal simulations of a 15kW three-phase application shows that poly-crystalline diamond tile can increase active converter power density from 13kW/kg to 17kW/kg when operating at a coolant flow rate of 6 liters per minute and a maximum junction temperature of 150°C. This is due to reduced ripple current in the output current and smaller heatsink size. Simulation results also show that predicted gravimetric power density is highly sensitive to the cooling system and its limits thermal limits. Simulations show for high junction-to-case temperatures, the gravimetric power densities for both modules are identical. Therefore, diamond substrates would only benefit power electronic converters which either have a low junction-to-case differential temperature or applications where higher switching frequencies are required, such as network facing converters, where there is an advantage of increasing switching frequency achieve potential weight savings in the output filters.

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