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Conductance Quantisation in patterned gate $In_{0.75}Ga_{0.25}As$ structures up to $6\times(2e^2/h)$

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Abstract

We present electrical measurements from $In_{0.75}Ga_{0.25}As$ 1-dimensional channel devices with Rashba-type, spin-orbit coupling present in the 2-dimensional contact regions. Suppressed backscattering as a result of the time-reversal asymmetry at the 1-dimensional channel entrance results in enhanced ballistic transport characteristics with clear quantised conductance plateaus up to $6\times(2e^2/h)$. Applying D.C. voltages between the source and drain ohmic contacts and an in-plane magnetic field confirms a ballistic transport picture. For asymmetric patterned gate biasing, a lateral spin-orbit coupling effect is weak. However, the Rashba-type spin-orbit coupling leads to a g-factor in the 1-dimensional channel that is reduced in magnitude from the 2-dimensional value of 9 to ~ 6.5 in the lowest subband when the effective Rashba field and the applied magnetic field are perpendicular.

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1. Introduction

The limitations of conventional electronic devices can be overcome by implementing spin-based electronics where the spin degree of freedom plays the central role [1]. Ballistic transport in semiconductor nanowires is essential for applications in quantum logic devices [2] and utilising electron spin to encode logical information also paves the way for quantum computing [3]. However, many challenges must be overcome, such as injection, manipulation and detection of spin-polarised currents. For this to be achieved, materials with high spin-orbit coupling are being investigated as this is a possible mechanism for spin control without ferromagnetic contacts or large applied magnetic fields. Rashba-type spin-orbit coupling [4-6] could achieve electrical spin control and generation of spin-polarised current without the use of ferromagnetic contacts [7]. The Rashba spin-orbit coupling effect arises when an electron moves (with in plane wave vector components k_x, k_y) in an asymmetric potential at a heterojunction interface with Rashba coefficient (α). An effective magnetic field exists, $\mathbf{B_R} = \frac{2\alpha(\mathbf{k_y}, -\mathbf{k_x}, 0)}{\mathbf{g^*}\,\mu_B}$ where μ_B is the Bohr Magneton and g* is the effective g-factor. This effective field lies in the plane of the 2-dimensional electron gas (2DEG) and is perpendicular to k. The precession of the electron spin can be modulated by adjusting the gate voltage to tune the confinement potential and hence α associated with the heterojunction. $In_xGa_{1-x}As$-based materials are ideal to study spin effects as the band structure is dominated by Rashba spin-orbit coupling induced by structural inversion asymmetry (SIA) at zero magnetic field [8]. The low electron effective mass (m*) of 0.040 m_e (m_e is the free electron mass, see reference [9]) in $In_{0.75}Ga_{0.25}As$ also results in high electron mobilities and large 1-dimensional subband energy spacing. These characteristics make this material system a promising candidate for ballistic spintronics devices in 1-dimension.

Patterned gate devices that define a quantum wire in the 2DEG system are an effective way to study 1-dimensional transport, from a picture of non-interacting states [10, 11] to many body effects driven by electron-electron interaction [12]. Conductance quantisation has been demonstrated in high mobility GaAs devices, yet the small effective g-factor (|g*|=0.44) and weak spin-orbit coupling make it difficult to observe spin-polarisation

phenomena without the application of an external magnetic field. The g-factor for $In_xGa_{1-x}As$ devices with $x > 0.5$ is $|g^*| \sim 8$ and for the case of $In_{0.75}Ga_{0.25}As$ $|g^*| = 9.1 \pm 0.1$ [13]. A summary of the initial spin transport measurements on undoped $In_{0.75}Ga_{0.25}As$ quantum wells and 1-dimensional channels were published in reference [14].

The outline of this article is as follows. The methods of fabricating and measuring the devices are described in Section 2. We then introduce the device characterisation and properties of 1-dimensional conductance in Section 3. We measure the device conductance when a D.C. voltage is applied to the source and the drain ohmic contacts and outline the method of obtaining an effective g factor in Section 3 C. In Section 4 the experimental data is summarised.

2. Methods

Standard Hall bars were processed from modulation doped, high electron mobility transistor (HEMT) structures. Au-Ge-Ni ohmic contacts were deposited using thermal evaporation and annealed at 450 ^oC for 120 s. The patterned gates were fabricated using electron beam lithography with Ti/Au metallisation. The device had a mobility of 2.9×10^5 $cm^2/V.s$ (at a carrier density of 2.3×10^{11} cm^{-2}) in the dark and 4.3×10^5 $cm^2/V.s$ (at 3.7×10^{11} cm^{-2}) after brief in-situ illumination at 4.2 K. Studies on modelling [15] the mobilities in the $In_{0.75}Ga_{0.25}As$ wafers used in this work have taken into account four different scattering mechanisms, background impurities, remote (modulated doped) impurity, alloy disorder and interface roughness scattering. It was found that alloy disorder becomes more important as the carrier density increases before the on-set of intersubband scattering at carrier density of $> 3.7\times10^{11}$ cm^{-2}. The patterned gates have a length (L) of 200 nm and a width (W) of 400 nm. The gates are insulated from the $In_{0.75}Al_{0.25}As$ barrier with 50 nm of SiO_2 dielectric. This is required as there is no Schottky barrier between metal gates deposited on the surface and the 2DEG [16]. The patterned gate devices were measured in a dilution fridge with a base temperature of 50 mK. Figure 1 shows the conductance on cooling from 4.2 K to 50 mK as the patterned gate voltage is swept to 0 V from depletion. An A.C. voltage of 100 μV was applied between the source and the drain during cool down. The device was briefly illuminated at

4.2 K in order to get a conductance (G) of 1000 μS. This corresponds to an electron density of 3.7×10^{11} cm^{-2}.

3. Experimental results and discussion

A. Device initialisation

In order to observe ballistic conductance quantisation the width of the channel must be comparable to the Fermi wavelength and the temperature must be low compared to the characteristic energy spacing of the 1-dimensional subbands in the channel. The electron mean free path (λ) which is 2.3 μm at 2.3×10^{11} cm^{-2} must be >> L, the channel length. Background impurities can lead to scattering in the channel and quasi-ballistic transport. In previous work [17] telegraph noise was identified as causing the conductance to vary by steps of ~ e^2/h in etched InAs quantum point contacts with a low mobility of 65×10^3 $cm^2/V.s$. The background impurity density in the wafer studied here is ~ 5.6×10^{15} cm^{-3} [15] which results in an average impurity spacing of ~ 60 nm and narrow patterned gate separations are needed to avoid the effects of quasi-ballistic transport. The effective potential profile of the 1-dimensional channel was shown to vary based on a study of 256 lithographically identical split-gates [18].

The strong spin-orbit coupling in these systems suppresses backscattering due to the weak anti-localisation effect [19] leading to enhanced conductivity and clear ballistic transport. This is demonstrated experimentally here where we observe quantised conductance up to $6\times G_o$ ($G_o = 2e^2/h$) see figure 1. A series resistance corresponding to the channel resistance at patterned gate voltage (V_{sg}) = 0 V, is removed to calculate the ballistic conductance of the channel. The conductance in figure 1 also shows a $0.7\times G_o$ structure which is widely accepted to be spin related [20, 21]. The $0.7\times G_o$ structure is more pronounced at 4.2 K [20] although the origin of the $0.7\times G_o$ anomaly is still unclear with explanations varying from ferromagnetic spin-coupling [22], to Wigner crystallisation [12] to the influence of inelastic scattering [23, 24].

B. Finite source drain voltage

Measurements were made at 50 mK with a D.C. source drain bias. This caused additional

plateaus to appear at half integer values $(N\pm1/2)\times G_o$ [25, 26] where N is an integer. However, the half integer plateaus reported here are significantly clearer than in the earlier studies and requires no external magnetic field [26, 27]. To fully investigate this phenomenon D.C. bias spectroscopy was performed on the device, stepping the D.C. bias (V_{sd}) from 8 mV to -8 mV in 0.025 mV increments. This can be seen in figure 2. A clear feature of this D.C. bias spectroscopy is the fact that it is asymmetric between positive and negative bias. While positive D.C. source drain bias has a $0.5\times G_o$ structure that stays strong with increasing D.C. source drain bias, there is a $0.25\times G_o$ structure that develops at negative D.C. source drain bias. This asymmetry could be from self-consistent electrostatic effects close to channel pinch-off, or it could be caused by lateral spin-orbit coupling due to a small asymmetry in the confining potential. This asymmetric appearance of the $0.25\times G_o$ could mean that a total spin polarisation is energetically unfavourable and a spin density wave or Skyrmion forms. Alternatively, a ferromagnetic ground state in an applied magnetic field with an interaction induced, spin-polarisation can be observed [28]. In GaAs devices under similar conditions a $0.25\times G_o$ plateau usually forms rather than at $0.5\times G_o$ and this has been explained as due to the source drain bias lifting the momentum degeneracy resulting in a unidirectional ferromagnetic order [29]. In this case a plateau appears at $0.5\times G_o$ and stays with increasing D.C. source drain bias. There are anomalous plateaus in the conductance that show up at $0.8\times G_o$ and $1.7\times G_o$ in the conductance plot, see figure 2 (b). These behave in a similar way to the $0.7\times G_o$ structure and are thought to be related to spin as a partially spin-polarized phase [30].

C. Applied magnetic fields

The magnetic field is applied in-plane and perpendicular to the effective Rashba field, i.e. along the 1-dimensional channel. This probes the low g-factor orientation and the effects of spin-orbit coupling should be clearer. 1-dimensional transport measurements [31] with an in-plane magnetic field show that in contrast to GaAs, only small magnetic fields are required to lift the spin degeneracy in InGaAs devices. Figure 3(a) shows a plot of the transconductance (dG/dV_{sg}) as the D.C. source drain bias is stepped from -8 mV to +8 mV in zero magnetic field. In figure 3(a) δV_g corresponds the difference in patterned gate voltage as the N = 2 and N = 1 subbands cross with finite V_{sd}. Figure 3(b) shows the

Zeeman splitting in the transconductance (dG/dV_{sg}) from 0 T to 8 T with V_{sd} = 0 V. In figure 3(b) δV_g corresponds the difference in patterned gate voltage as the N = 2 and N = 1 subbands cross in a parallel magnetic field. $In_{0.75}Ga_{0.25}As$ devices require ~ 1.5 T of parallel magnetic field ($B_{||}$) to lift the spin degeneracy compared with ~ 6 T for GaAs [31]. We obtain the g-factor using the technique developed in [26] which combines the measurement of the splitting due to the applied source drain bias with measurements where Zeeman splitting is due to the parallel magnetic field. The subband energy is measured by observing the splitting in gate voltage (δV_g) due to an applied D.C. source drain bias. The energy difference between spin-split energy levels is defined by the Zeeman energy (E_Z), see equation (1),

$$|\mathbf{g^*}| = \frac{1}{\mu_B}\frac{\mathbf{dE_Z}}{\mathbf{dB_{||}}} = \frac{\mathbf{1}}{\mu_B}\frac{\mathbf{dE_Z}}{\mathbf{dV_{sg}}}\frac{\mathbf{dV_{sg}}}{\mathbf{dB_{||}}} = \frac{\mathbf{e}}{\mu_B}\frac{\mathbf{dV_{sd}}}{\mathbf{dV_{sg}}}\frac{\mathbf{dV_{sg}}}{\mathbf{dB_{||}}} \qquad (1)$$

e is the unit of charge. In figure 3(a), the subband spacing is shown to be between 3.6 meV and 2.5 meV. Larger values were reported in $In_{0.75}Ga_{0.25}As/InP$ [32]. However, these devices were fabricated from etched wires that require a perpendicular magnetic field in order to reduce the disorder in the system and achieve quantised conductance [27, 33]. The term $dV_{sg}/dB_{||}$ can be estimated from figure 3(b). We obtain an effective g-factor of 6.5 for the lowest subband N = 1, and the data is obtained in the absence of Landau quantisation using finite perpendicular magnetic field. Table 1 is a summary for the lowest 3 subbands.

In a 2DEG with Rashba-type spin-orbit coupling, the band structure is split into two parabola, with a linear shift in k (the in-plane wave vector) with energies, $E^{\pm}(k)$ given by equation (2),

$$\mathbf{E^{\pm}(k)} = \frac{\hbar^2\mathbf{k}^2}{2\mathbf{m}^*} \pm \alpha\mathbf{k} \qquad (2)$$

where α is the Rashba parameter for this heterojunction system. In the $In_{0.75}Ga_{0.25}As$ quantum well, the Rashba coefficient is 0.67×10^{11} eV.m with a spin-orbit splitting energy

of ~ 2.2 meV [8]. When this Rashba spin-orbit coupling is included in the calculation of the effective g-factor, this reduces the estimated value to 6 in the lowest subband (N = 1) for in-plane applied fields perpendicular to the Rashba field. The reduction in g-factor from the measured 2-dimesnional value is due to the competition of Rashba and Zeeman magnetic fields. This reduction is one of the manifestations of the Rashba spin-orbit coupling effect that creates an effective magnetic field (~ 4 T), pinning the spin angular momentum in this in-plane direction [8].

D. Asymmetric patterned gate voltages

Asymmetric split-gate biasing was studied by stepping one patterned gate voltage and sweeping the second, see figure 4, where ΔV shows the difference in patterned gate voltage. We observe a weak spin-split $0.5\times G_o$ plateau appearing, however this feature increases to $0.75\times G_o$ as the channel is made more asymmetric. In addition there are plateaus which appear at $1.5\times G_o$ and $3.5\times G_o$ as the channel is made more asymmetric. The spin-split $0.5\times G_o$ plateau has already been observed in an InAs quantum well with InGaAs barriers, when the confining potential was made asymmetric. This was ascribed to a lateral spin-orbit coupling effect [34]. However these measurements reported in reference [34] were made using etched channels with side gates. The etched wires have edges that are exposed to roughness and disorder and the spin-orbit length is smaller due to stronger confinement [35]. Spin-polarisation can be triggered by lateral spin-orbit coupling and lead to fully spin-polarised state in the presence of strong electron-electron interaction however this effect is not seen in these structures even though the measured Rashba spin-splitting energy is ~ 2.2 meV in this 2-dimensional system [8].

4. Conclusions

$In_{0.75}Ga_{0.25}As$ patterned gate devices investigated in this paper show the effects of spin-orbit interaction predominantly through a g-factor reduction rather than spin resolved conductance plateau at $0.5xG_o$ and higher conductance half plateaus. These experiments have determined the optimum device length scales to study quantised conductance with minimal effects from disorder and impurities that have plagued early studies of devices based on the InGaAs material system. These experiments have demonstrated that

$In_{0.75}Ga_{0.25}As$ patterned gate devices are suitable for future spintronic devices that require only minimal applied magnetic fields. There is a reduction in backscattering due to spin-orbit coupling at the 1-dimensional channel that leads to enhanced ballistic quantisation up to a conductance of $6\times(2e^2/h)$ even with appreciable disorder present.

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Figure captions

Figure 1 The differential conductance (G) in units of $2e^2/h$ as a function of patterned (split) gate voltage (V_{sg}) from 4.2 K to 50 mK in intervals of 0.05 K for the device with channel length 200 nm and patterned gate separation 400 nm. The conductance has been corrected for a series resistance and offset horizontally by 25 mV per set temperature. The dashed blue line indicates the $0.7\times(2e^2/h)$ conductance feature.

Figure 2(a) D.C. bias spectroscopy of the device from 0 mV to 8 mV. The $0.5\times(2e^2/h)$ conductance plateau is observed and remains from 3 mV with further plateaus developing at 1.5, 2.5 and $3.5\times(2e^2/h)$. **(b)** D.C. bias spectroscopy of the device from 0 mV to -8 mV. The $0.5\times(2e^2/h)$ is again observed at ~ 3 mV, but tends to shift below $0.5\times(2e^2/h)$ to $0.25\times(2e^2/h)$ as the D.C. bias is increased.

Figure 3(a) The Transconductance (dG/dV_{sg}) as a function of gate voltage (V_{sg}) plotted against D.C. source drain bias (V_{sd}) with parallel magnetic field ($B_{||}$) set to 0. Regions of bright orange and red correspond to large amplitude dG/dV_{sg}, indicating the locations of subband transitions. **(b)** Transconductance (dG/dV_{sg}) as a function of gate voltage (V_{sg}) and parallel magnetic field ($B_{||}$). Regions of orange and red indicate large amplitude of dG/dV_{sg} corresponding to locations of subband transitions.

Figure 4 The device conductance as a function of asymmetric voltage to the patterned gates. One gate is held constant and the other gate is shifted incrementally up to ΔV = -2.8 V at 50 mK in voltage steps of 20 mV.

Figures

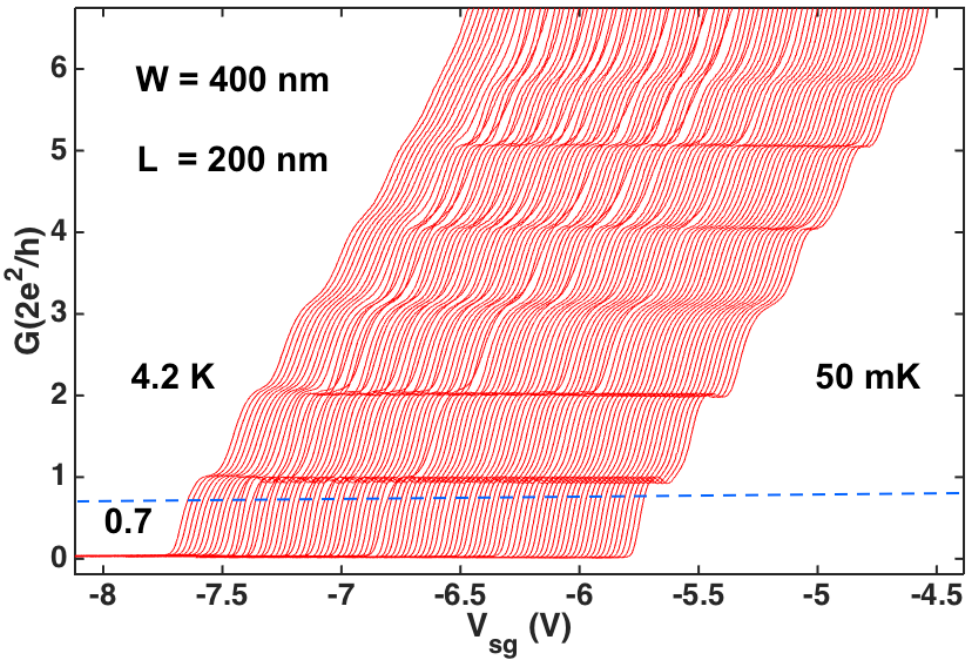

Figure 1.

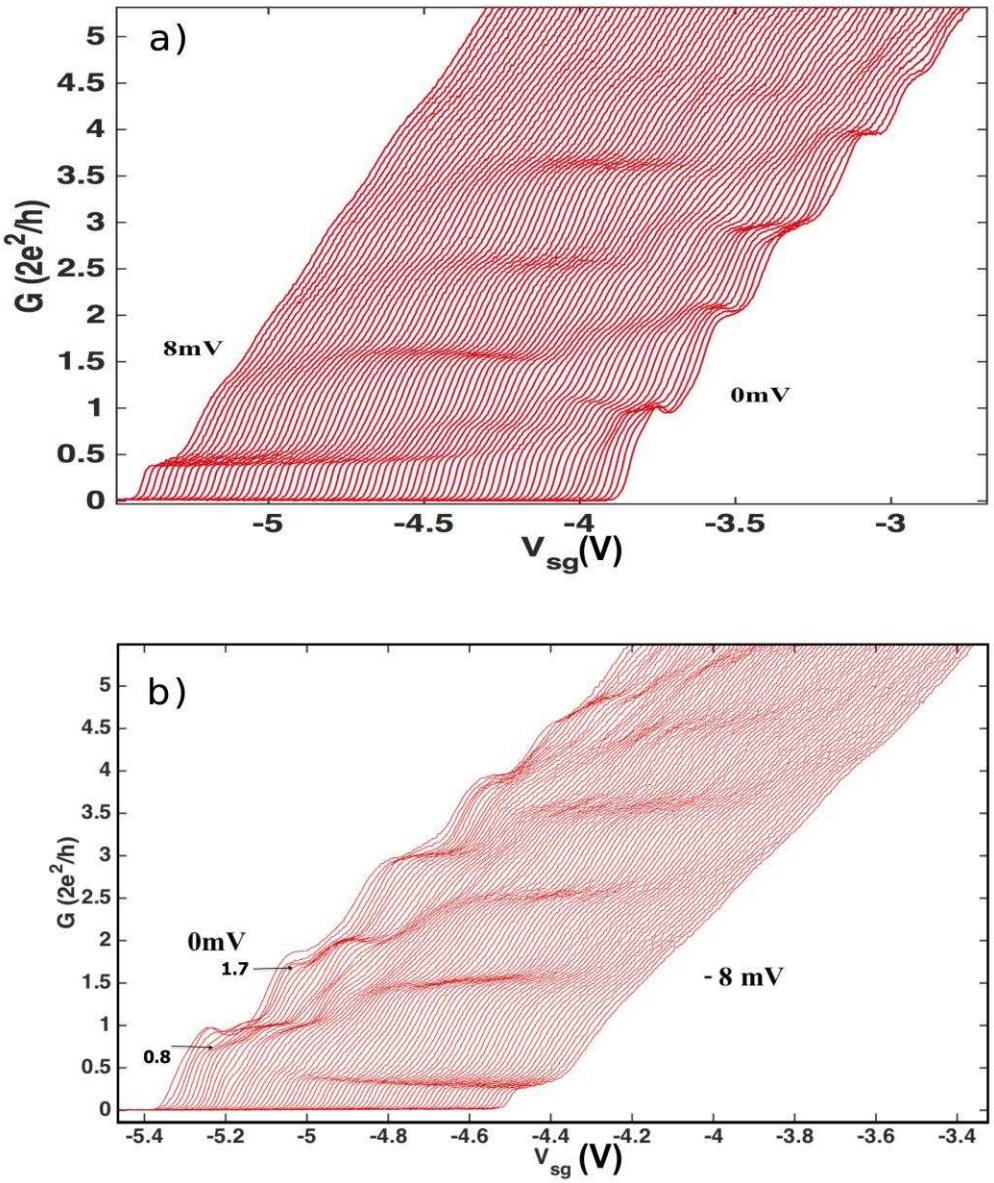

Figure 2.

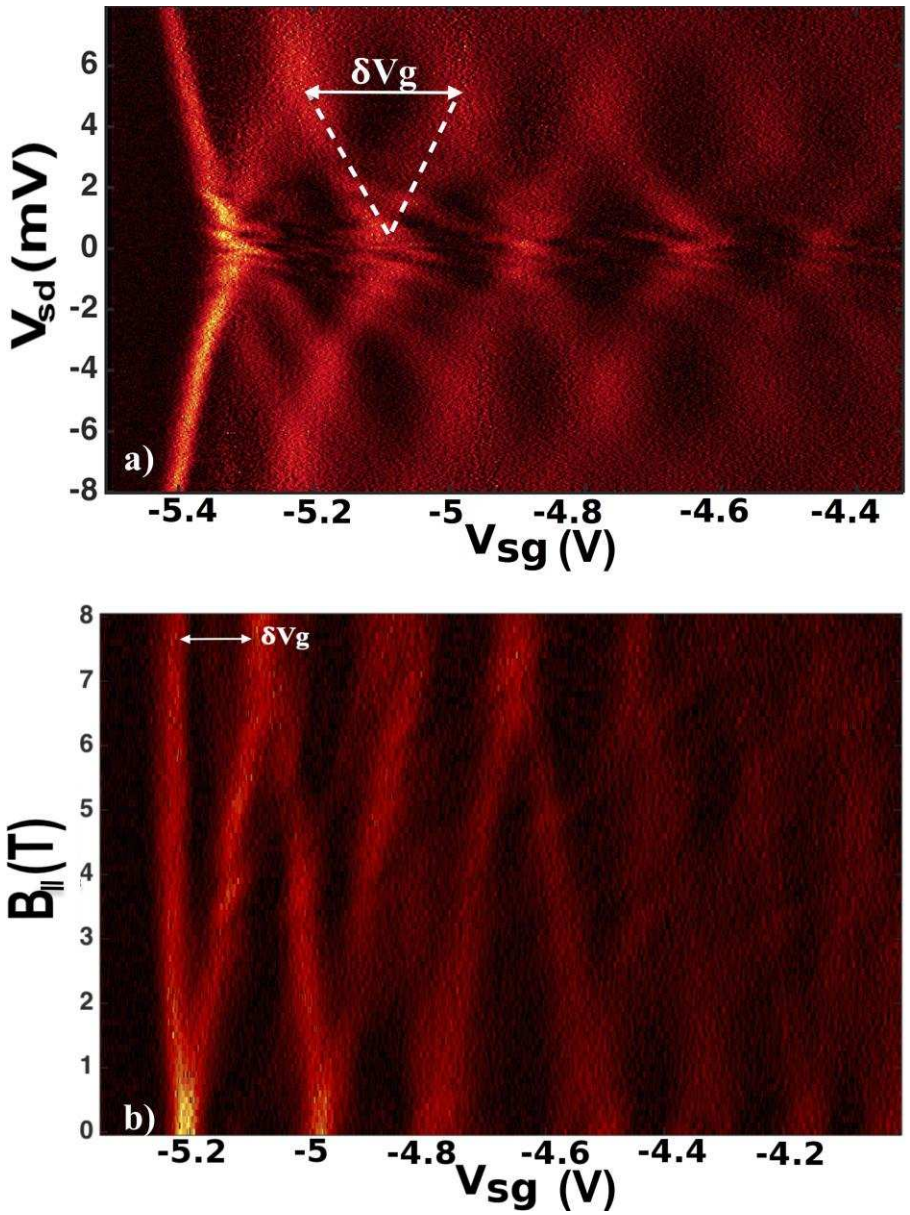
δVg
6
4
2
0
-2
-4
-6
-8
V_{sd} (mV)
a)
-5.4
-5.2
-5
-4.8
-4.6
-4.4
V_{sg} (V)
δVg
8
7
6
5
4
3
2
1
0
$B_{||}$(T)
b)
-5.2
-5
-4.8
-4.6
-4.4
-4.2
V_{sg} (V)

Figure 3.

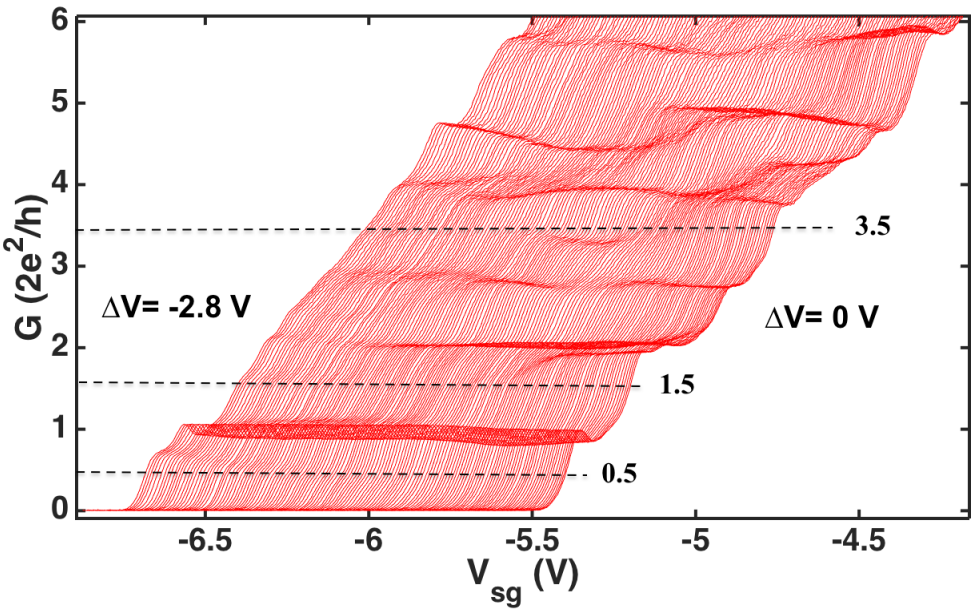

Figure 4.

Tables

subband	**N=1**	**N=2**	**N=3**
$\delta E_{n,n+1}$ (meV)	3.8	2.9	2.5
$\delta V_g/\delta B_{\parallel}$ (V/T)	0.016	0.021	0.022
$\delta eV_{sd}/\delta V_g$ (meV/V)	23	17.1	12.8
$\lvert g^* \rvert$	6.5	6.2	4.9

Table 1. Summary of the g-factors obtained for the first three sub-bands