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PLL controller for achieving zero-voltage switching (ZVS) in inductorless half-bridge drive piezoelectric transformer resonant power supplies

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Abstract: Inductorless half-bridge, piezoelectric transformer (PT) resonant power supplies require careful control if zero-voltage switching (ZVS) of the MOSFETs is to be achieved. Here, the authors describe how a phase-locked loop (PLL) may be used to achieve this by ensuring adequate deadtime exists between the two MOSFETs to allow the PT input voltage to fully charge to the DC link. Experimental results demonstrate the operation of the system.

1 Introduction

Piezoelectric transformers (PTs) use mechanical vibration coupling between their input (primary) and output (secondary) sections to convert between voltage levels. PTs offer many potential advantages over conventional wound transformers including high-power density (>40 Wcm^{-1}) [1], low EMI, reduced weight, high galvanic isolation and improved efficiency [2]. They are typically constructed using hard piezoelectric materials such as lead-zirconium titanate (PZT), and so they typically exhibit a strong resonant peak. This resonant behaviour has led to the development of power supply circuits wherein the magnetic transformer and inductor components in a conventional supply are completely replaced by the PT. PTs are already found employed in back-lighting power supplies for laptop computers, PDAs and LCD TVs [3], fluorescent and LED lighting [4], mobile phone battery chargers [5] and ionisation and plasma generators [6].

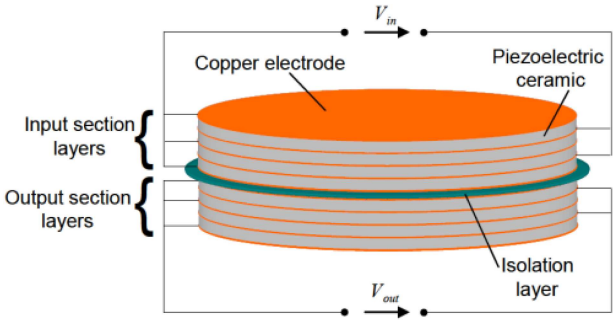

Fig. 1 *Typical radial mode PT*

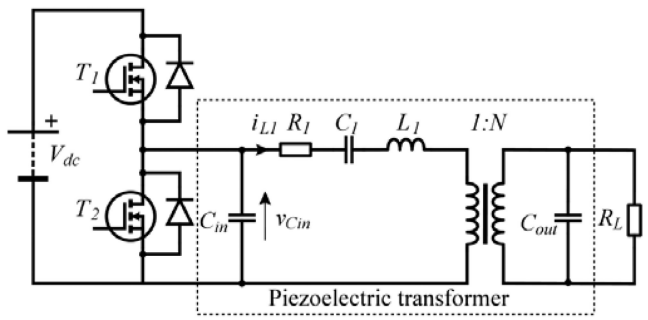

Fig. 2 *Mason equivalent circuit model of a PT*

The input and output capacitances of a PT can be relatively large, and they need to be specifically designed if they are to achieve zero-voltage switching (ZVS) without the use of a series inductor, thus ensuring low volume and low cost from the supply. A critical design criterion for achieving ZVS in inductorless half-bridge driven piezoelectric transformer-based power supplies was described in [7], where it was shown that ZVS could be achieved if the ratio between the input and output capacitance was kept below a specific level and the deadtime was set to 90° when driving the PTs at resonant frequency and operating with a matched load.

Here, we use a phase-locked loop (PLL) control system to lock on to PTs the resonant frequency establishing a fixed phase relationship between the resonant current and half-bridge voltage. The necessary deadtime value of 90° is then generated to achieve ZVS.

2 Piezoelectric transformer power supplies

Piezoelectric transformers are multi-layered ceramic devices consisting of an input section (similar to a primary winding) and an output section (the secondary winding equivalent). Fig. 1 shows an example of a radial mode PT wherein each layer is a disc of the PZT material.

Although PTs can be constructed in different ways to achieve step-up and step-down ratios, they are generally characterised by the Mason equivalent circuit about their primary resonant mode (Fig. 2). The input capacitance C_{in} and output capacitance C_{out} correspond to the input and output terminal electrode capacitances, respectively; L_1, C_1 and N model the acoustic mechanical resonant phenomenon; and R_1 represents the effects of mechanical damping and other losses. The half-bridge MOSFETs T_1 and T_2 are operated in anti-phase at a specific frequency. The deadtime is inserted between a commutation event to prevent shoot through and to provide sufficient time for the PT input voltage to charge between the DC rails.

During a single half-cycle, the circuit can exist in one of only three possible circuit configurations or modes:

M1: Both MOSFETs are off and v_{Cin} is being charged by i_{L1}.
M2: T_1 (or T_2) is on and v_{Cin} is clamped to V_{dc} (or to 0 V).
M3: v_{Cin} has exceeded V_{dc} (or fallen below 0 V) and the anti-parallel diode of the MOSFET is conducting.

Fig. 3*a* shows the typical waveforms for a PT achieving ZVS where the PT input voltage v_{Cin} exceeds the DC link voltage.

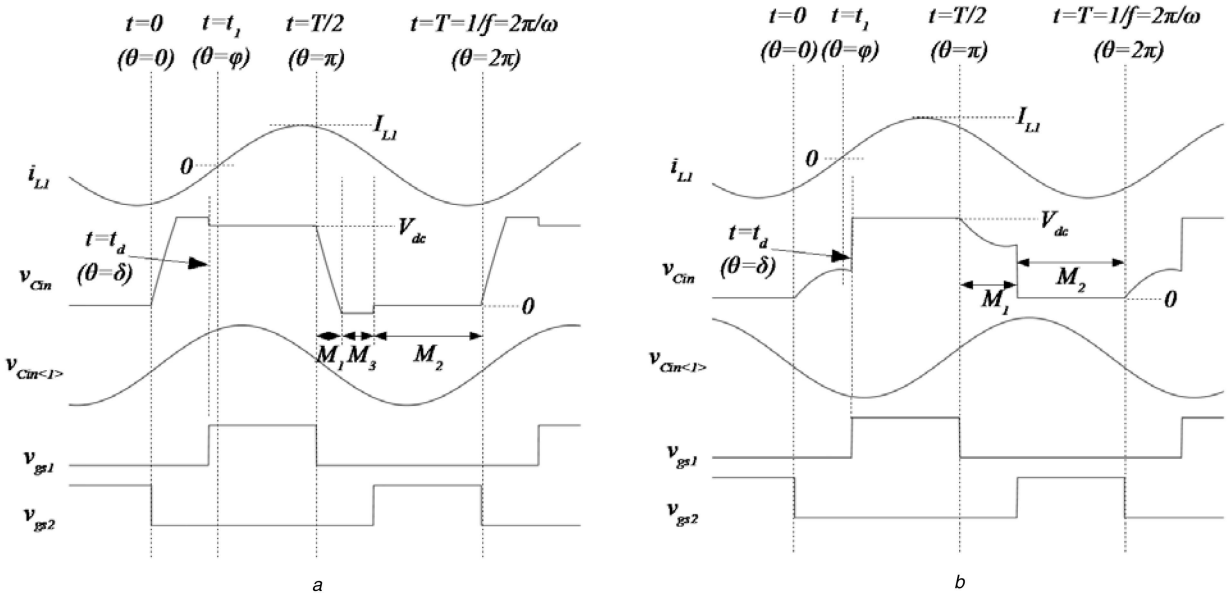

Fig. 3 *Half-bridge waveforms for PT inverter*
(a) With ZVS, ***(b)*** Without ZVS

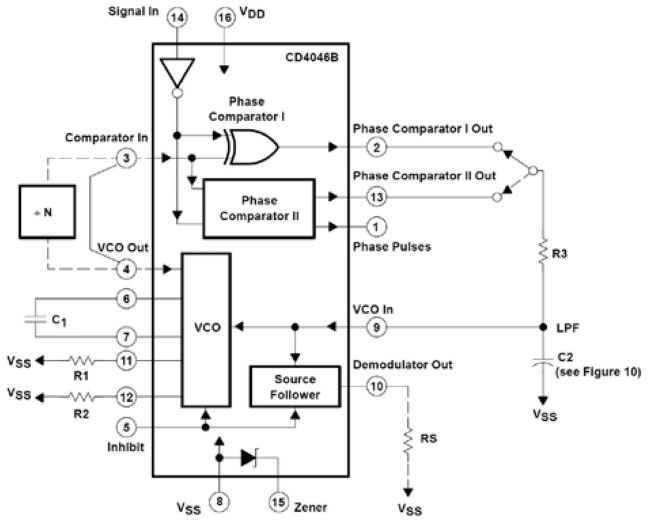

Fig. 4 *Block diagram for 4046 PLL [8]*

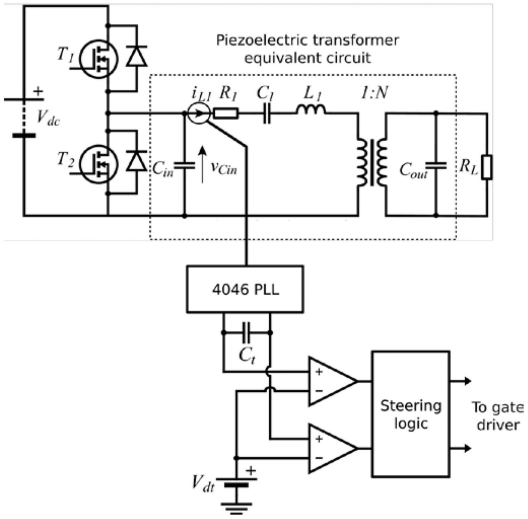

Fig. 5 *Block diagram of the proposed controller*

Fig. 3*b* shows the case where ZVS is not achieved. In this situation, v_{Cin} undergoes an abrupt change in voltage, leading to increased switching losses.

In [7], we developed a critical design criterion that states ZVS can always be achieved if the input-to-output capacitor ratio meets the inequality $C_{in}/(NC_{out})<0.636$ and the deadtime is set to 90° when operated at the resonant frequency. In this work, we use a PLL to lock on to the resonant frequency and some simple logic to generate the deadtime waveform.

3 Description of PLL controller operation

A CMOS 4046 PLL is at the heart of the proposed ZVS controller. The 4046 PLL contains a voltage controlled oscillator (VCO) and two phase comparators. Referring to Fig. 4, R1, R2 and C1 set the operating frequency range of the VCO. Phase comparator II is a phase–frequency detector (PFD) and allows the PLL to synchronise to both the frequency and the phase of the input signal presented on pin 14. Thus, when locked, the VCO out signal on pin 4 is locked in phase and frequency to the input signal on pin 14.

The proposed PLL ZVS control system is shown in Fig. 5. The 4046 PLL locks on to the frequency and phase of the resonant current i_{L1}. The voltage across the PLL timing capacitor v_{Ct} is seen to be a triangular waveform, and this voltage acts as a reference waveform for the phase offset comparator. The MOSFET gate drive signals are generated by comparing v_{Ct} to a fixed reference voltage V_{dt}, scaled to represent the required 90° phase shift and then using appropriate steering logic.

4 SPICE simulation model and results

To validate the performance of the proposed PLL controller, a model of the system was implemented in LTSPICE, as shown in Fig. 6. The voltage-controlled oscillator operates by charging a timing capacitor (shown as C1) via a constant current source. When the voltage on the capacitor reaches $V_{logic}/2$, the current reverses and the capacitor is charged in the opposite direction. Two current sources are used: a fixed source representing the minimum current and a variable source representing the VCO input signal. An H-bridge, consisting of switches S1–S4, is used to reverse the current flow through the timing capacitor. Voltage-controlled switches S5–S6 are comparators and generate pulses (p1 and p2) for the R–S flip–flip that controls the VCO H-bridge. The VCO output signal is node c ('Q' on gate A1), and this signal is frequency- and phase-locked to the resonant current.

The PFD is implemented using D-type flip–flops. The input to the PFD is the sign of the resonant current (behavioural source B1) and is connected to the clock input of A3. The VCO output is connected to the clock input of A4. The RC networks on the outputs of the flip–flops provide a short time delay to help avoid

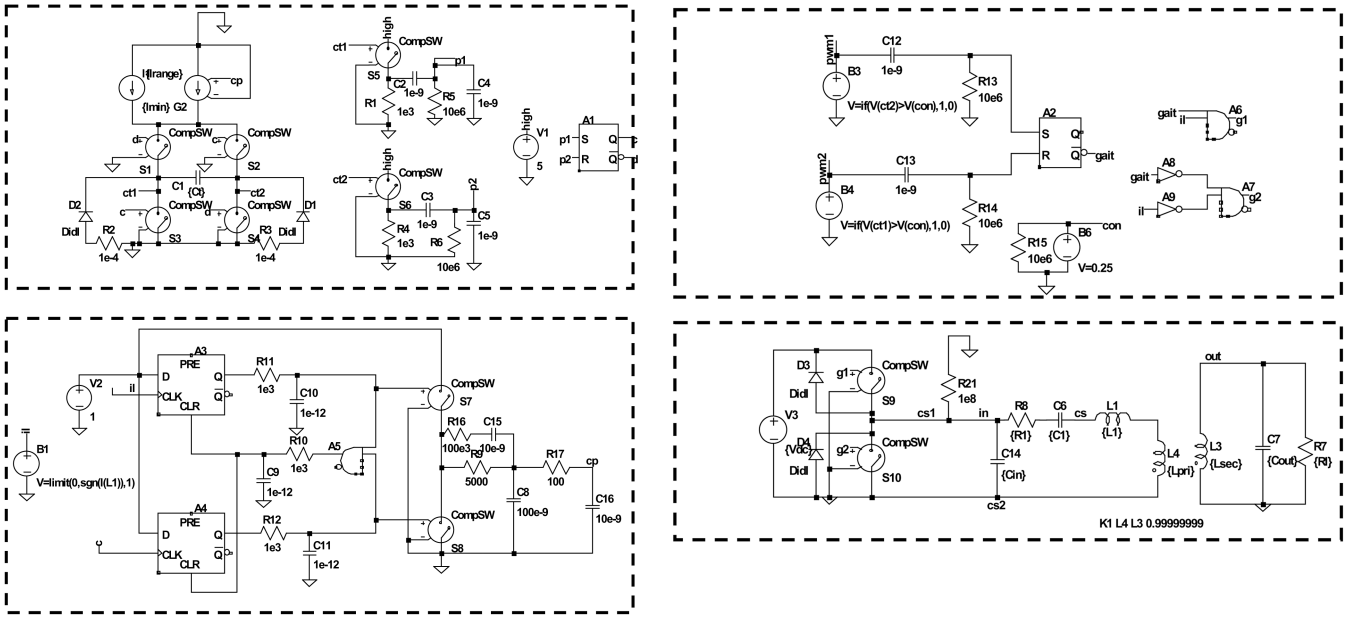

Fig. 6 *LTSPICE model for the PLL PT control system*

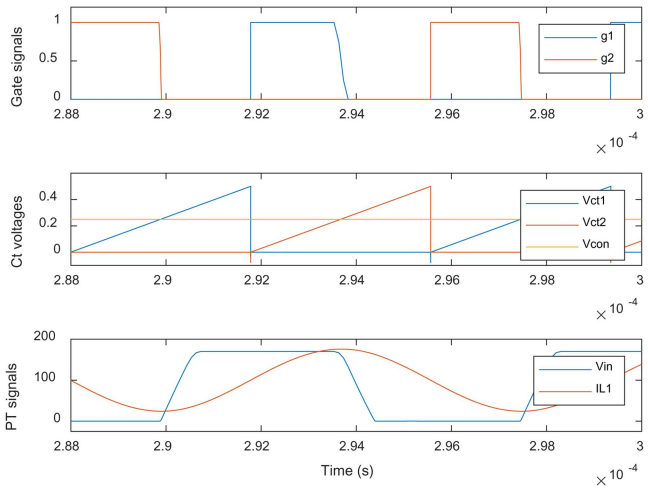

Fig. 7 *PLL control circuit waveforms*

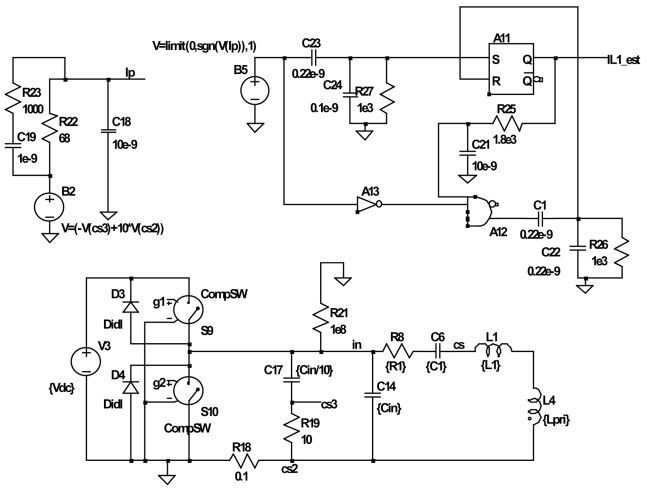

Fig. 8 *Current estimator circuit*

convergence issues. Switches S7–S8 are the charge-pump switches that charge/discharge the RC network (loop filter). Voltage cp is the output voltage from the PFD, and this is signal-fed to the VCO, thereby allowing the PLL to lock on to the resonant current i_{L1}.

The gate drive logic section takes the PLL signal (c) and time capacitor waveforms and generates the gate drive control signals for the half-bridge switching devices. Behavioural sources B3–B4 are comparators and generate a pulse when $V_{Ct} > V_{logic}/4$ (shown as 0.25 V). Since there is one pulse for the positive half-cycle and another for the negative half-cycle, an R–S flip–flop is used to generate the 90° phase-shifted signal (shown as gait). Combinational logic is then used to generate the actual half-bridge gate drive signals featuring the required 90° deadtime interval.

Fig. 7 shows the simulation waveforms from the LTSPICE model. The upper plot shows the gate drive signals for the half-bridge switches (g1 and g2). As can be seen, these signals are locked to the resonant current and provide the required 90° deadtime to achieve ZVS. The middle plot shows the timing capacitor waveforms V_{Ct1} and V_{Ct2} along with the comparator reference signal. As can be seen, each voltage has a maximum value of 0.5 V (LTSPICE internal logic voltage is 1 V). V_{ct2} provides the positive half-cycle reference for the gate drive comparator. The lower plot shows the PT input voltage and the resonant current with ZVS clearly achievable.

5 Practical issues

In practice, the resonant current i_{L1} cannot be measured directly as it is internal to the PT. However, it can be estimated from the PT input current and PT input capacitor current using the technique described in [9]. Fig. 8 shows an LTSPICE implementation of the current estimator wherein R18 senses in the PT input current and R19 senses a scaled version of the input capacitor current. The two current signals are combined using behavioural voltage source B3. Since the estimated current signal contains noise and switching edges, an R–S flip–flop (A11) with delays is used to improve noise immunity.

6 Experimental results

Measurements from a practical implementation of the proposed control circuit are shown in Fig. 9. CH1 is the estimated resonant current, and the waveform marked M is the resonant current obtained using the oscilloscope's Math function. CH3 and CH4 are the input capacitor current and PT input current, respectively. CH2 is the PT input voltage. The result clearly shows that ZVS has been achieved.

7 Conclusion

This paper has described a control system for achieving ZVS in piezoelectric transformer-based power supplies. Using a PLL, the controller locks on to the resonant frequency and is able to maintain a 90° deadtime period between the half-bridge gate

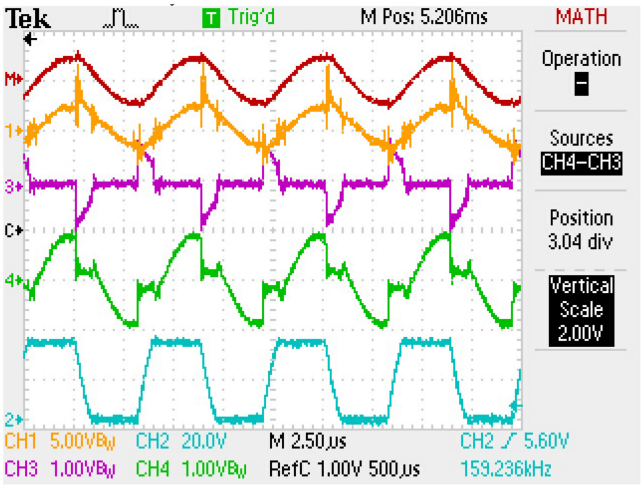

Fig. 9 *Experimental waveforms taken from the prototype controller*

signals. The operation of the system has been described, and an LTSPICE simulation model of the CMOS 4046 based PLL controller has been given. Experimental results have shown that the proposed control is capable of maintaining ZVS operation.

The control as described does not provide output voltage regulation, and it is suggested that a bang-bang-type control system be used to regulate the output voltage if this functionality is required.

8 Acknowledgments

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