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Micro Electronic Systems via Multifunctional Additive Manufacturing

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Micro Electronic Systems via Multifunctional Additive Manufacturing

Abstract

Purpose – This paper aims to demonstrate the innovative functionality of additive manufacturing technology provided by combining multiple processes for the fabrication of packaged electronics.

Design/Methodology/Approach – This research is focused on the improvement in resolution of conductor deposition methods through experimentation with build parameters. Material dispensing with two different low temperature curing isotropic conductive adhesive materials were characterised for their application in printing each of three different conductor designs, traces, z-axis connections and fine pitch flip chip interconnects. Once optimised, demonstrator size can be minimised within the limitations of the chosen processes and materials.

Findings – The proposed method of printing z-axis through layer connections was successful with pillars 2mm in height and 550µm in width produced. Dispensing characterisation also resulted in tracks 134µm in width and 38µm in height allowing surface mount assembly of 0603 components and thin-shrink small outline packaged integrated circuits. Small 149µm flip chip interconnects deposited at a 457µm pitch have also been used for packaging silicon bare die.

Originality/Value – This paper presents an improved multifunctional additive manufacturing method to produce fully packaged multilayer electronic systems. It discusses the development of new 3D printed, through layer z-axis connections and the use of a single electrically conductive adhesive material to produce all conductors. This facilitates the surface mount assembly of components directly onto these conductors before Stereolithography is used to fully package multiple layers of circuitry in a photopolymer.

Keywords Additive Manufacturing, Process Integration, DLP Stereolithography, Material Dispensing, Multilayer Embedded Electronics, Flip Chip Packaging

Paper Type Research Paper

Introduction

Electronics manufacturing techniques require a wide range of materials including conductors and dielectrics to generate complex circuitry. These processes are characteristically wasteful and their template driven nature requires volume production to achieve economic viability. This results in long pre-production timescales and a lack of customisation and versatility.

Additive Manufacturing (AM) technologies, commonly termed 3D printing, have been introduced as an innovative alternative to a variety of traditional manufacturing technologies (Sharma 2014)(Anon 2012). They provide benefits such as waste reduction, increased geometric freedom and digitally driven fabrication directly from a CAD model, making templates and moulds obsolete. Until recently, AM research and development has been focused on individual processes and materials, therefore adopting their inherent limitations. To encourage 3D printing technology to reach its full potential, multiple processes area being combined to create functional products from numerous materials. Favourable characteristics of AM techniques can be combined with a range of material possibilities to provide increased functionality in an array of applications (Lipson & Kurman 2013) such as microfluidics, embedded sensor systems and electronic packaging.

A variety of AM processes have been hybridised to challenge traditional electronics manufacturing technologies including combinations of both ultrasonic consolidation (A. J. Lopes et al. 2006) and stereolithography (Lopes et al. 2012) with direct writing.

A concept was introduced for the encapsulation of a printed circuit board (PCB) within a package fabricated using stereolithography (Niese et al. 2014). Off-axis vias were added to the package to route power to the PCB, and were to be created using the Additive 3D Molded Interconnect Device (ADDMID) process. Laser processing of the doped photopolymer resin allows ablated structures to be metallised through the exposure of coated aluminium particles.

The fabrication of electronics using a hybrid stereolithography and direct writing approach was first proven by The University of Texas at El Paso, who first demonstrated the compatibility between conductive materials and photopolymer materials (Palmer et al. 2004). Photopolymer substrates with trenches and off-axis tunnels were fabricated using a top down laser based stereolithography technique. Through hole components were placed in trenches which were then filled with liquid photopolymer and cured, leaving a network of channels on the surface to contain the conductive ink (A. Lopes et al. 2006). Direct write technologies were used to deposit low viscosity conductive inks into the channels and the ink was also pumped into the tunnels, allowing conductive channels to cross without intersection. Conductive traces were deposited in channels and components housed in individual trenches on the substrate surface. The compatibility of this approach with surface mount technology is limited, resulting in a larger electronic footprint and in addition, the production of circuitry was restricted to the surface of the part with specific structural features required to control conductor deposition.

Aerosol jetting has been applied to the printing of conductors on 3D printed plastic surfaces. In 2012, Fused Deposition Modelling and aerosol jetting were interleaved by Optomec and Stratasys to print functional strain gauges and conductors to generate electric power for the propeller engine of an unmanned aerial vehicle (Paulsen et al. 2012). Circuitry with a resolution of 10µm was produced onto three dimensional surfaces however, this process was again limited to post processing of a pre-fabricated substrate.

Voxel8 released a hybrid system combining both Fused Filament Fabrication (FFF) and dispensing within one material extrusion machine in 2016 (Borghino 2015). This allows the simultaneous printing of substrates and electronic circuits to produce functional electronic structures. The resolution of the FFF process is typically limited to 0.8mm features in the x and y axes due to the 0.4mm diameter nozzle and suffers from stair stepping issues in the z-axis due to the large layer thicknesses. Despite the advantages of the multi-material process the dimensional capabilities of the system are limited by the choice of processes.

In this paper a manufacturing process combining direct light projection (DLP) based Stereolithography (SL) and direct write (DW) technology is presented, allowing the production of fully functional multilayer electronic systems directly from a digital model. This combination of manufacturing techniques coupled with mid-process cleaning, electronic surface mount component assembly and thermal curing provides the multi-material, multi-process functionality required to produce high quality, high density electronics packaged in geometrically complex structures.

Hybrid Manufacturing Process, Apparatus and Materials

Manufacturing Process

The manufacturing process chain has been detailed in Figure 1. It begins with substrate fabrication via bottom up DLP Stereolithography, creating a base in a layer-by-layer build method. After ultrasonic agitation to remove excess liquid photopolymer, isotropic conductive adhesives (ICAs) are selectively dispensed onto the clean substrate surface to simultaneously produce conductive tracks, surface mounted device (SMD) interconnects and novel z-axis through layer connections in the form of freestanding pillar structures. Surface mount component assembly is then conducted onto deposited interconnects before exposure to a low temperature in a thermal oven to cure the ICA without degrading the substrate material. Finally, the electronics are embedded through a single long period of exposure to a projected UV image, resulting in small protrusions of pillar tips through the layer as well as providing a flat surface for subsequent electronic dispensing. Stages (b) to (e) in

Figure 1 can be repeated multiple times to produce a fully packaged multilayer electronic system (Figure 1(h)).

Figure 1. Overview of the multifuctional additive manufacturing process

Stereolithography System

Digital light projection (DLP) Stereolithography (SL) is an Additive Manufacturing (AM) process that fabricates three dimensions parts from a liquid photopolymer by selectively curing multiple thin layers of material one on top of the other (Hull 1986). This method differs from laser based Stereolithography processes as the photopolymerisation is achieved by exposing a single layer of photosensitive resin to a projected image for a predetermined period of time. DLP projection can be orientated downwards or upwards, the latter has been utilized in this integrated process. A projection system is positioned underneath the vat with a transparent base and antistiction polydimethyl-siloxane (PDMS) coating, with the projection lens positioned and focused on the centre of the base. This method builds parts upside down, producing a surface high quality surface finish as it is polymerised in contact with the PDMS layer (Zhou et al. 2013).

A mUVe 1.5 DLP system from mUVe3D was modified to improve its structural rigidity, allowing the process to be paused, parts removed and, reinserted in an identical location. A 405nm ultraviolet projection source, DLP Lightcrafter™ 4500 projection module from Texas Instruments, was added with a resolution of 109µm over a 140mm x 87mm projection area. The light density of the projector was measured at 3.16mW/cm^2 at the lens, and an average of 0.98mW/cm^2 at the point of interaction with the photopolymer using an International Light IL1400A UV light meter. The single-wavelength ultraviolet light source reduced the stresses on the substrates caused by absorption of a wide range of wavelengths emitted from a white light source. Manual micrometre height control of the build platform height was incorporated ensuring that the layer thickness was kept constant and the home position could be accurately altered. This bespoke DLP Stereolithography apparatus with bottom up UV projection orientation was used to produce the base photopolymer substrates with a layer thickness of 100µm. To produce a complex package, geometrically intricate external walls can be fabricated creating a cavity to contain the layer of deposited circuitry. Once the SLA build stage has finished, the part can be subjected to ultrasonic agitation in a solvent, removing all excess uncured photopolymer before being dried by a clean compressed air source.

Liquid Photopolymer Materials

Liquid photopolymers are all sensitive to light however, different photoinitiators can change the wavelength of light to which the material is sensitive. To initiate polymerisation the energy of light

exposure must breach the activation energy of the initiator (Andrzejewska 2001)(Gruber 1992). Traditional, commercial laser based SL systems contain high power 365nm lasers and therefore, commercial resins are designed to polymerise when exposed to this wavelength and intensity of light. The integration of a 365nm light source into a DLP projector resulted in too low an intensity. A 405nm light source in the form of a Texas Instruments DLP Lightcrafter™ 4500 Evaluation Module was used. MakerJuice SF resin from MakerJuice Labs was selected for its low stress behaviour under UV light and heat exposure, its visible clarity and high resolution capability.

Dispensing System

Dispensing is one of a variety of direct writing methods by which conductors can be deposited onto a photopolymer surface. A Musashi Shotmaster500 dispensing system capable of high resolution automated movement was used to deposit silver filled conductive materials. The pneumatic pressure produced by the Musashi SuperΣCMII digital control dispenser makes it compatible with high viscosity materials, therefore facilitating the printing of high load silver filled materials to produce conductors. In addition, the process is fully digitally driven with dedicated MuCAD software enabling the design and control of dispensing patterns, machine movement and printing parameters. This system is capable of printing at speeds between 0.1mm/s and 300mm/s and pressures between 30kPa and 500kPa which, when combined with regulation of nozzle size, print gap and material characteristics, make this process highly controllable. Traditionally z-axis connections in electronics manufacturing are produced by a combination of subtractive and additive methods. Through the use of AM a hole can be fabricated layer by layer without subtractive machining methods however; the method of encapsulation introduced in this paper prevents the creation of a deep, high resolution via holes. A novel method of connecting multiple layers of circuitry was therefore developed resulting in three dimensional, freestanding pillars that could be embedded, leaving a 50µm peak exposed to contact subsequent layers of circuitry. These z-axis through-layer connections were deposited simultaneously with conductive tracks and SMD interconnects in one automated process.

Conductive Materials

Epotek® E4110-PFC and EJ2189 silver filled ICAs with maximum particle sizes of ≤20µm and ≤45µm were selected for experimentation for three reasons. Firstly, they cure at low temperature, below the glass transition temperature of the photopolymer substrates, secondly, they have a high viscosity, ensuring the deposition can be controlled and structures will maintain their desired shape and finally, can be used to produce all conductors simultaneously in these embedded structures. These material properties are listed in Table 1. Both candidate epoxies can be thermally cured at temperatures ranging from room temperature (23°C) to 150°C, however, the liquid photopolymer limitedthis curing temperature to a maximum of 100°C before the substrate degraded. However,

due to the lower glass transfer temperature Tg of cured SL resin (MakerJuice SF) the curing temperature of both conductive epoxies was limited to 100 °C. Any higher curing temperature resulted in the SL substrate degrades that caused cracking and partial delamination of the very top surface.

Table 1. Important properties of chosen conductive materials according to Epotek specifications

Electronic Packaging

The use of isotropic conductive adhesive materials to fabricate conductors makes this dispensing process and materials compatible with surface mount assembly (SMA). SMA is the most commonly used packaging method for mounting components directly onto printed circuit boards due to its high density capability, high throughput and low cost. Components can be placed directly onto dispensed ICA interconnects. The final stage in the deposition of electronics is low temperature thermal curing. A regime of 80°C for 3 hours was used to prevent degradation of the substrate, resulting in an approximate volume resistivity of $7x10^{-4}$Ωcm in both materials. According to Table 1, when both conductive epoxies are fully cured, their resistivity should be less than 5 mΩ cm. The experimental samples measured resistivity was in this expected range.

The SL apparatus is used to package each circuit layer individually. With or without a cavity, embedding of electronics is conducted by re-inserting the build platform with attached specimen into the material vat, pressing the top 100µm of the pillars into the non-stick PDMS layer and flood exposing the thick layer of photopolymer. To prevent the formation of bubbles in the cavity, it is filled facing upwards, the air is left to settle out and the wetted part is then inserted into the SL apparatus. This process can then be repeated creating multiple embedded layers in a geometrically complex package. The thickness of these layers is determined by the height of the tallest components and therefore layers 2mm and 1.2mm in thickness were proposed for 1206 and 0603 (imperial code) surface mount devices.

Packaging can also be conducted on a chip scale. Figure 2 shows the difference between the traditional and AM methods of flip chip packaging daisy chain patterned bare die, the example used in this feasibility test. Flip chip packaging allows bare microchips to be attached face down onto a substrate with a smaller pitch between the array of bond pads facilitating a higher input/output density. This technique is an evolution of SMA and reduces substrate weight in addition to making the device thinner. Conventional copper tracks and solder bumps can be replaced with ICA filled channels in the substrate and printed interconnects. In addition the photopolymer is used to fully encapsulate the chip acting as both the insulating underfill and package.

Figure 2. Comparison of flip chip packaging via a) conventional methods and b) multifuctional additive manufacturing

Photopolymers substrates were fabricated with surface trenches before being cleaned and filled with isotropic conductive adhesive. Once cured, the surface was planarised using a polishing process before fine pitch interconnects were deposited onto each end of the sub-surface trenches. Alignment of the interconnects with metallised tracks and pads on the underside of the chip can was conducted using a Leica Wild M3Z optical beam splitting microscope with manual micrometre alignment before a rotating placement arm was used to place the chip in position.

Development and Experimental Miniaturisation of Conductors

To facilitate the shrinking of the footprint of electronic systems produced using AM methods, the density of printed conductors required increasing. Systematic experimentation of different dispensing parameters was conducted to determine the combination required to produce the smallest uniform traces and z-axis connecting pillars. The miniaturisation of these systems was also reliant on the compatibility of this dispensing process with smaller surface mount components and integrated circuits, requiring the pitch of dispensed features to be reduced.

The selected ICA materials were the limiting factor in this investigation, with their maximum particle sizes limiting the inner diameter (ID) of the nozzles through which they could be deposited. There is a rule of thumb from ICA suppliers that the nozzle diameter should be 5 times larger than the maximum particle size to avoid any clogging. For Epotek® E4110-PFC, the maximum particle size was 20µm (Table 1), and thus the nozzle ID was limited to 100µm. 200µm and 250µm ID nozzle were also utilised in this work for comparison.

Conductive Tracks

Three printing parameters were identified as having the greatest influence on the track profile, specifically the width as it is the most influential parameter for the reduction of the dispensing pitch and therefore miniaturisation. An array of tracks was produced using two epoxies and a combination of three experimental variables, nozzle inner diameter, printing pressure and print speed. A range of suitable printing pressures for material A (100kPa to 450kPa) and material B (30kPa to 180kPa) and, print speeds (1mm/s to 7mm/s) were determined during a preliminary investigation. Values outside these ranges resulted in poor track quality, lack of wetting to the substrate or an excessive volume of deposited material. An Alicona InfiniteFocus® G4f non-contact variation focus microscopy system with a x10 object lens was used to scan the profile and extract trace height, width and cross sectional area.

Track widths resulting from deposition in material A were analysed and are presented in Figure 3(a). In addition, Figure 3(b)-(d) presents a matrix of track profiles showing the effect of print parameters on their appearance. Smaller track widths and heights were achieved by reducing nozzle ID, decreasing print pressure and increasing print speed however, to print material A through the narrowest 100µm nozzle, a minimum print pressure of 250kPa was required. The narrowest uniform trace was produced using a nozzle ID of 100µm, printing pressure of 300kPa and speed of 7mm/s and, measured 170µm in width and 43µm in height. By comparison, the 200µm and 250µm IDs resulted in minimum trace widths of 304µm and 352µm.

Figure 3. Effect of printing parameters on track width and appearance of material A

Material B exhibited the same behaviour however, due to its lower viscosity, printing pressures ranged between 30kPa and 90kPa and, trace width increased at a greater rate with pressure as shown in Figure 4(a).

A comparison of Figure 4(b)-(d) with the material A track matrix shows that trace profiles produced in material A are smoother than material B. This has been attributed to its higher viscosity resulting in less solvent evaporation during thermal curing and its smaller particle size. Tracks of the same height printed in both ICAs demonstrated that material A produced samples up to 20% narrower than material B due its higher viscosity however, a larger pressure was required that may result in larger volumes of material deposited. Material B was able to produce the smallest track profile with a width of 134µm and height of 38µm, realised through a 100µm nozzle orifice using a pressure of 140kPa and speed of 7mm/s. The lower viscosity material separates more easily from the nozzle orifice and in combination with a lower printing pressure, allowed smaller volumes of ICA to be deposited.

Figure 4. Effect of printing parameters on track width and appearance of material B

Z-axis through Layer Conductors

Minimising the footprint of the z-axis interconnects is contingent on a compromise between the base diameter and the stability of the structure. With increasing base diameter, the achievable height of the pillar increases. Preliminary testing was conducted to design the tool path and dimensions of the pillars and, identifies the limits of print speed and pressure. Individual design files with dimensions proportional to each nozzle ID, shown in Figure 5, were produced to allow the aspect ratios of printed structures to be compared to one another.

Figure 5. Freestanding pillar designs for each nozzle ID

The freestanding nature of these z-axis interconnecting pillars required a high aspect ratio to be achieved. A comparison of the height, diameter and aspect ratio of pillars produced using the two candidate ICAs is presented in Figure 6. Structures printed through 250µm and 200µm nozzle IDs resulted in material A pillars on average 32% (~2mm) and 15% (~1.7mm) higher than material B. Pillar diameters are similar at lower pressures however, these diameters increase more rapidly with pressure in material B, peaking with a difference in diameter of 28% with the 250µm nozzle and 13% with the 200µm nozzle which, when combined with the pillar heights, create higher aspect ratios in material A structures.

Figure 6. Diameters, height and aspect ratios of pillars produced in materials A and B using 250µm and 200µm nozzle IDs

Following this preliminary investigation material B was discounted for use in pillar dispensing due to its slumping behaviour which is exaggerated by higher volume deposition and the weight of sequentially stacked layers. Experimentation with material A was undertaken to identify the relationship between nozzle size, dispensing speed and dispensing pressure on the height and diameter of pillars measured using an Alicona InfiniteFocus® G4f non-contact variation focus microscopy system. With an experimental mandate to minimise the diameter of the pillars and ensure enough height to connect circuit layers a maximum acceptable value of base diameter was set at 1mm. Figure 7(a) and (b) shows the effect of changing nozzle ID, print speed and printing pressure on the diameter and height of printed pillars. The visual effect of decreasing pressure, nozzle ID and print speed on pillar appearance are also shown in Figure 7(c)-(e). Diameter increases quickly with pressure however, as the height is largely determined by the design height, it only increases by small increments due to the higher volume of deposited material. In addition, increasing speed reduced both the track width and the height. Finally, larger nozzles also resulted in higher volume deposition and therefore wider and taller conductors.

Figure 7. Graphic representation of effect of changing printing parameters on a) diameter and b) height of profiles produced with decreasing c) pressures, d) nozzle sizes and e) print speeds

The highest aspect ratio achieved during this investigation was 2.26 at a height of ~1.5mm and diameter of ~0.67mm using a 200µm nozzle ID at a pressure of 80kPa and print speed of 7mm/s. The 100µm nozzle produced the smallest pillar base diameter of ~0.5mm however with a height of

~0.7mm the aspect ratio is limited to 1.4. This characteristic would therefore prevent this structure from forming a connection through the 1.2mm thick embedding layers proposed for packaging of 0603 surface mount devices without additional layers added to the design.

Additional iterative experimental changes to the height of the pillar design were made to create the tallest structure possible with a maximum diameter of approximately 1mm. Using the more viscous material A and a 250µm nozzle ID, printing pressure of 90kPa and print speed of 4mm/s, a height of 3.8mm and width of 0.9mm was achieved over 16 printed layers. A maximum of 18 layers could be printed through a 200µm nozzle and 24 were achieved through a 100µm nozzle. Figure 8 summarises these results and shows a comparison with material B.

Figure 8. Comparison of largest achievable pillar structures using a combination of two materials and three nozzle sizes

Material A and a 100µm nozzle ID produced the narrowest pillar diameter whilst measuring over 2mm in height. Although its measured aspect ratio, 3.67, is smaller than its 250µm nozzle equivalent, 3.81, packages were designed with a maximum 2mm layer thickness therefore making the 100µm nozzle most suitable as it produced the narrowest pillar diameter while meeting the height requirement.

Interconnect Dispensing for Flip Chip Packaging

The miniaturisation of electronic packaging is contingent on the integration of smaller packaging technology with this multifuctional additive manufacturing process, facilitating the demonstration of chip scale packaging. This required the deposition of interconnecting conductive bumps onto photopolymer substrates at a narrow pitch. Interconnect features were achieved by locating the nozzle at a designed location, with a given print gap and pressure and, dispensing was actuated for a pre-determined period of time. The resulting bumps were then scanned using the Alicona microscope to analyse the topography. Preliminary experimentation provided a range of pressures, print gaps and actuation times for both materials through a 200µm nozzle. The achievable feature sizes of the two epoxies were compared at a 0.3 second actuation time and 100µm print gap to determine their suitability for this process. Figure 9(a) shows that feature diameters 100µm narrower have been achieved using material B, a result of the lower viscosity and therefore lower pressure required to print these features. Pressure values below the minimum shown are either a restriction of the dispensing system or result in no material flow. Material A displays greater error and printing inconsistency, demonstrating sub-optimal results for use in chip scale packaging.

Material A also produces higher, sharper peaks shown in Figure 9(b), resulting in a greater chip standoff distance and a higher volume of dispensed material, therefore making material B more suitable.

Figure 9. Comparison of interconnects printed in materials A and B

Figure 10 shows the systematic investigation of material B over a range of pressure actuation times to determine the optimum parameters for the production of the smallest possible consistently deposited feature. The smallest diameter produced through the 200µm nozzle was 259µm while this dimension was reduced to 149µm through a 100µm nozzle. The smallest ICA bumps were produced at a print gap of 60µm with values both above and below resulting in insufficient adhesion to the substrate and increased spreading of the epoxy respectively.

Figure 10. Relationship between printing pressure, actuation time and bump diameter at a 60µm print gap with a 100µm nozzle in material B

Interconnects with a diameter of 150µm showed high repeatability, proving that the production of fine pitch interconnects is possible using additive manufacturing technology and therefore facilitating the combination of this deposition technique with substrate manufacturing methods.

Demonstrators

Multilayer 555 Timer

A flashing 555 timer circuit was chosen to demonstrate the capability of this multi-process manufacturing technique for embedded electronics. The three layer design was incorporated into a pyramid to exhibit the potential of this technique to develop packages with higher geometric complexity. Figure 11 presents the iterative miniaturisation of this three layer demonstrator as a result of the dispensing process characterisation and reduction in SMD and IC dimensions. The two examples show a reducing substrate base width from 30mm x 30mm to 15mm x 15mm made possible by decreasing the footprint of the electronics from 12mm x 12mm to 8mm x 8mm.

Figure 11. Comparison of demonstrator size reduction across three iterations

Figure 11(a) and (b) demonstrate the 50% reduction in size of surface mount devices (from 1206 package to 0603 package) and packaging of a 4.4mm x 3mm x 1.2mm thin-shrink small outline package (TSSOP) with a pitch of 650µm between pins, condensed from a 4.9mm x 3.9mm x 1.75mm mini small outline package (MSOP) with a pitch of 1.27mm between pins. This facilitated the reduction in embedding layer thickness from 2mm to 1.2mm. The dispensing parameters also changed resulting in the use of a 100µm nozzle to produce circuitry on the smaller substrate while a 250µm nozzle had previously been used to produce the larger iteration.

Flip Chip Packaging

A 6.3mm x 6.3mm daisy chain bare die with pre-bumped metallised pads was packaged using multifuctional additive manufacturing techniques. Ideally these pads would not have solder on them as it increases the standoff height and contact resistance however, a polishing process was used to remove the majority of the solder to more accurately simulate the packaging of a bump-free chip. The pads are 195µm x 195µm with a pitch of 457µm and alternate pairs connected by a track. An inverse of this pattern is required on the substrate to create a complete electrical daisy chain connection. This inverse pattern was produced by printing a pattern of 600µm x 200µm x 200µm trenches in the substrate surface, filling the trenches with ICA, thermally curing the conductive material and finally, surface planarization. Interconnect features are then deposited at each end of the filled trenches with a pitch of 457µm, the result of which is shown in Figure 12(a). A bonding pressure of 8g was used before an additional thermal curing stage is conducted to cure the chip in place Figure 12(b) and (c). The chip can then be packaged using an identical embedding method to that presented in Figure 1, creating a fully encapsulated chip an example of which is shown in Figure 12(d).

Figure 12. Stages of flip chip packaging by multifuctional additive manufacturing

A four point probe was used to measure the contact resistance of interconnects via redistribution channels fabricated in the photopolymer substrate. An average resistance of 2.3Ω was obtained between measurement pads with no change measured after the embedding and under filling process.

This flip chip packaging capability could be applied to the bottom layer of circuitry printed in complex substrates and embedded using the same method, allowing the photopolymer to act as an insulating underfill material protecting the chip itself and corresponding interconnects from external

mechanical stresses acting on the substrate itself. This demonstrates the high resolution capability of this hybrid process in its application to the packaging of electronic circuitry on a chip scale.

Conclusion

A novel method for the production of multilayer embedded electronics by integrating additive manufacturing processes has been presented. DLP projection based stereolithography is used to manufacture an electronic substrate onto which conductors can be printed in an isotropic conductive adhesive. Surface mount electronic devices can subsequently be mounted on the ICA interconnects before they are thermally cured and packaged through an additional photopolymerisation stage.

A unique approach to the fabrication of z-axis through layer connections has been introduced, characterised and proven through the production of multiple demonstrators over two and three layers. Experimentation has shown that these freestanding pillars can be printed over a maximum of 16 layers with an aspect ratio of 3.81. A combination of increasing print density of conductors and an increasing number of circuit layers alongside detailed print parameter investigation has facilitated the reduction in circuit footprint from 12mm x 12mm to 8mm x 8mm. The size of surface mount electronics and therefore, embedding layer thickness have also been halved.

Demonstrators have been produced proving the use of integrated additive manufacturing technologies to create complex polymer structures with fully functioning internal multilayer electronics in the form of a flashing 555 timer circuit. The same encapsulation process has been applied to flip chip packaging, with dispensing of fine interconnect feature diameters as small as 259µm at a pitch of 457µm.

This technology has proven its potential to produce intricate electronic systems embedded within complex packages using a unique combination of additive manufacturing processes. Its digitally driven nature makes it ideal for iterative development of both its shape and function exhibiting its suitability for a variety of application areas including electronics packaging, lab on chip and condition monitoring.

Future Recommendations

The resolution of this process is limited by the particle size of commercially available low temperature isotropic conductive adhesive materials. The formulation of an ICA with smaller particles would allow the use of smaller nozzle IDs for dispensing and therefore a further reduction in size of conductors. This improvement in combination with the current DLP SLA process would result in a significant reduction in electronic footprint of embedded multilayer systems.

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Table 1. Important properties of chosen conductive materials according to Epotek specifications

	Epotek E4110-PFC (Material A)	Epotek EJ2189 (Material B)
Max. Particle Size (µm)	≤20	≤45
Viscosity (cPs)	50000-60000	55000-90000
Thixotropic Index	3.3	5.2
Curing Regimes	1hr @ 120°C 3hr @ 80°C 6hr @ 45°C	15min @ 150°C 1hr @ 100°C 3hr @ 80°C 72hr @ 23°C
Volume Resistivity (Ωcm)	$\leqslant 5x10^{-3}$	$\leqslant 5x10^{-3}$

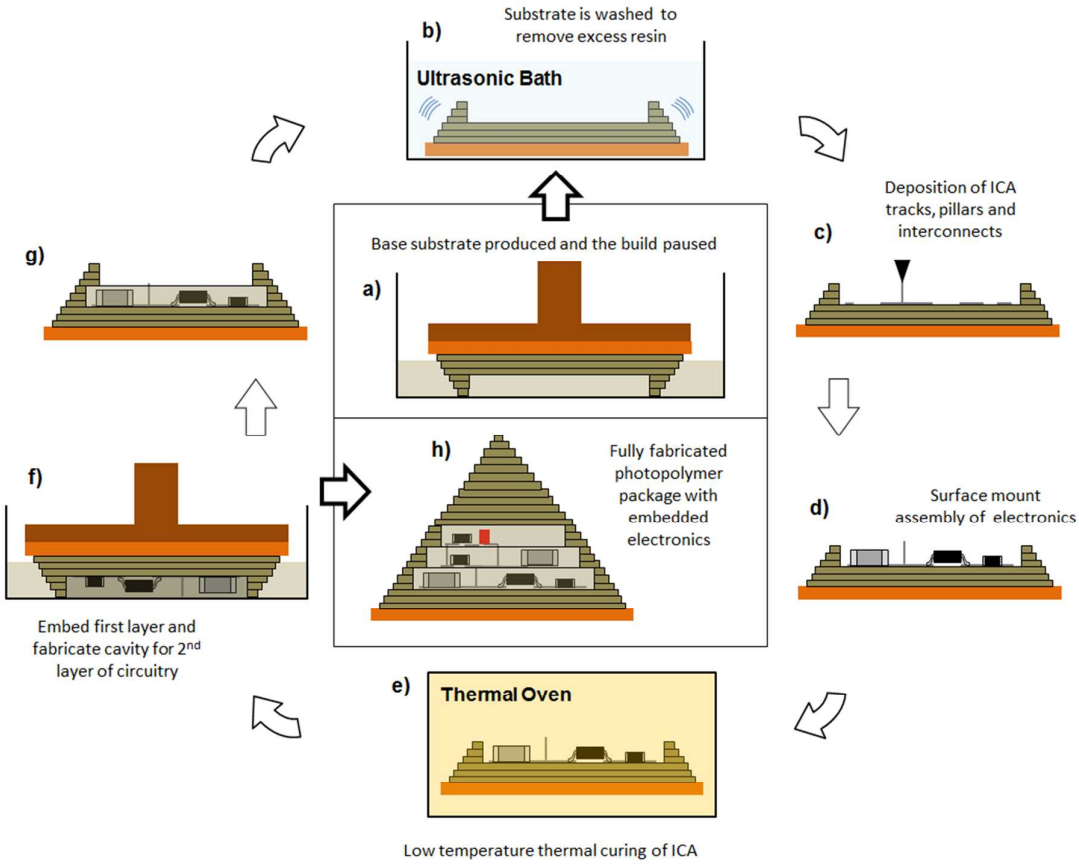

Figure 1. Overview of the hybrid additive manufacturing process

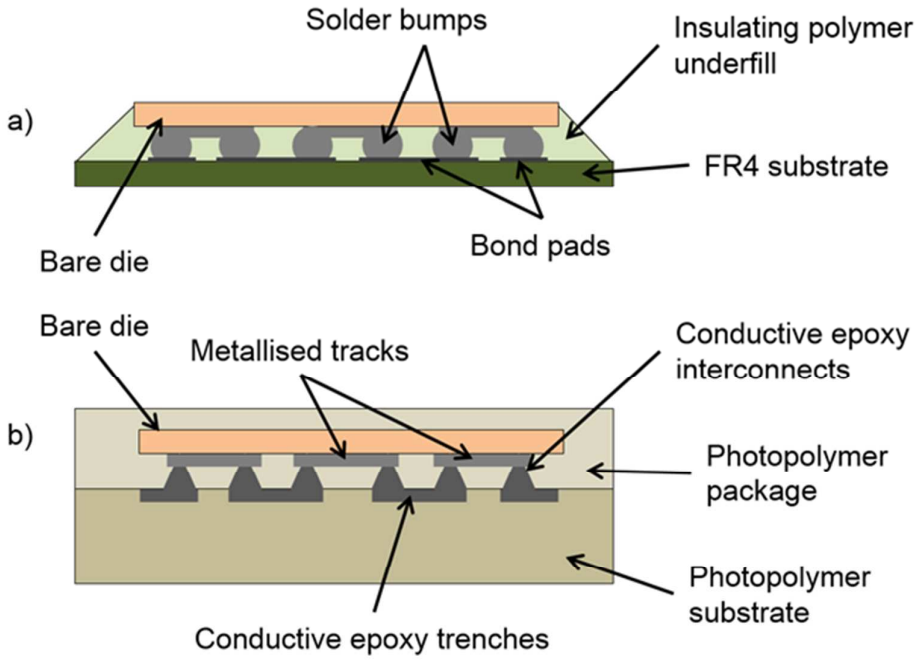

Figure 1. Comparison of flip chip packaging via a) conventional methods and b) hybrid additive manufacturing

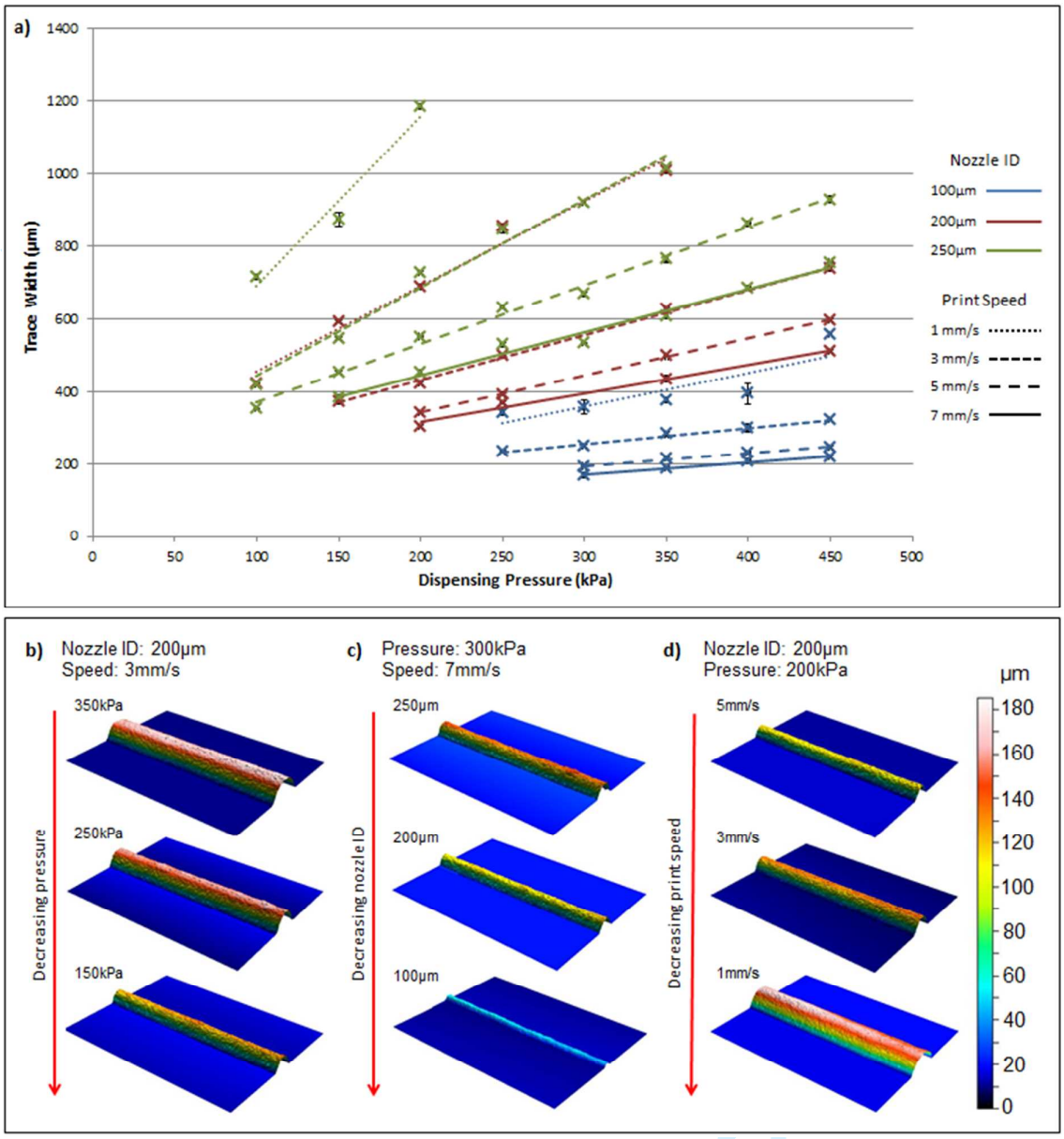

Figure 1. Effect of printing parameters on track width and appearance of material A

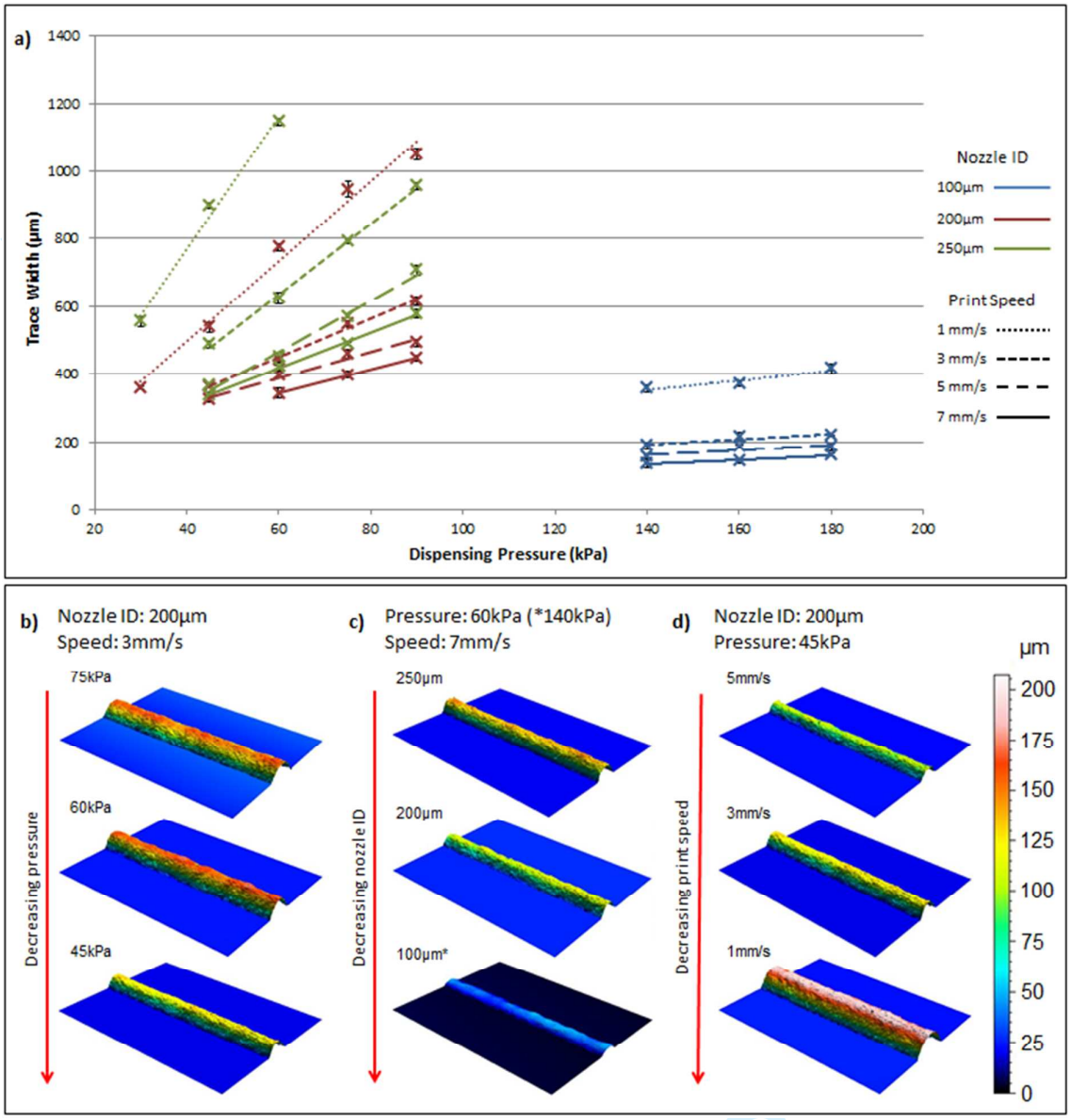

Figure 1. Effect of printing parameters on track width and appearance of material B

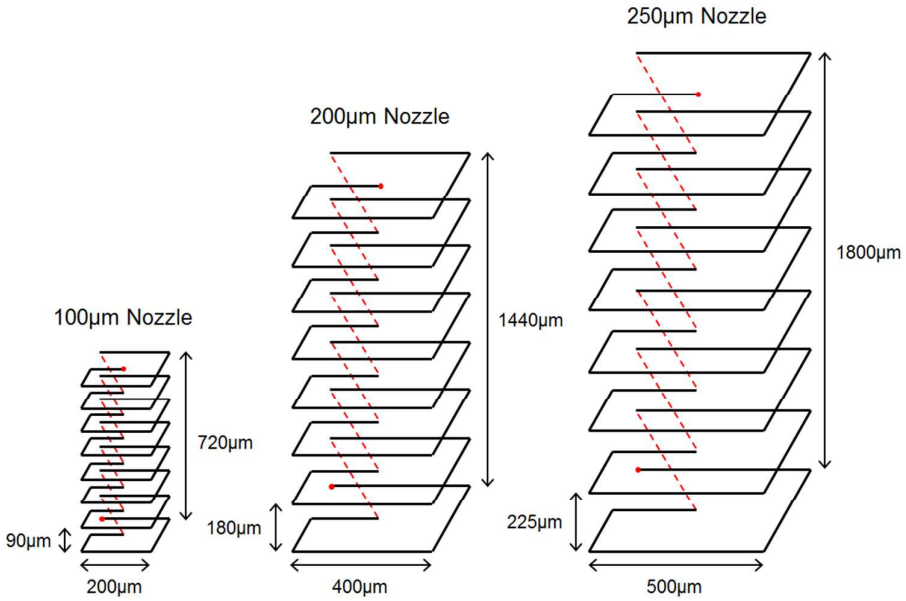

Figure 1. Freestanding pillar designs for each nozzle ID

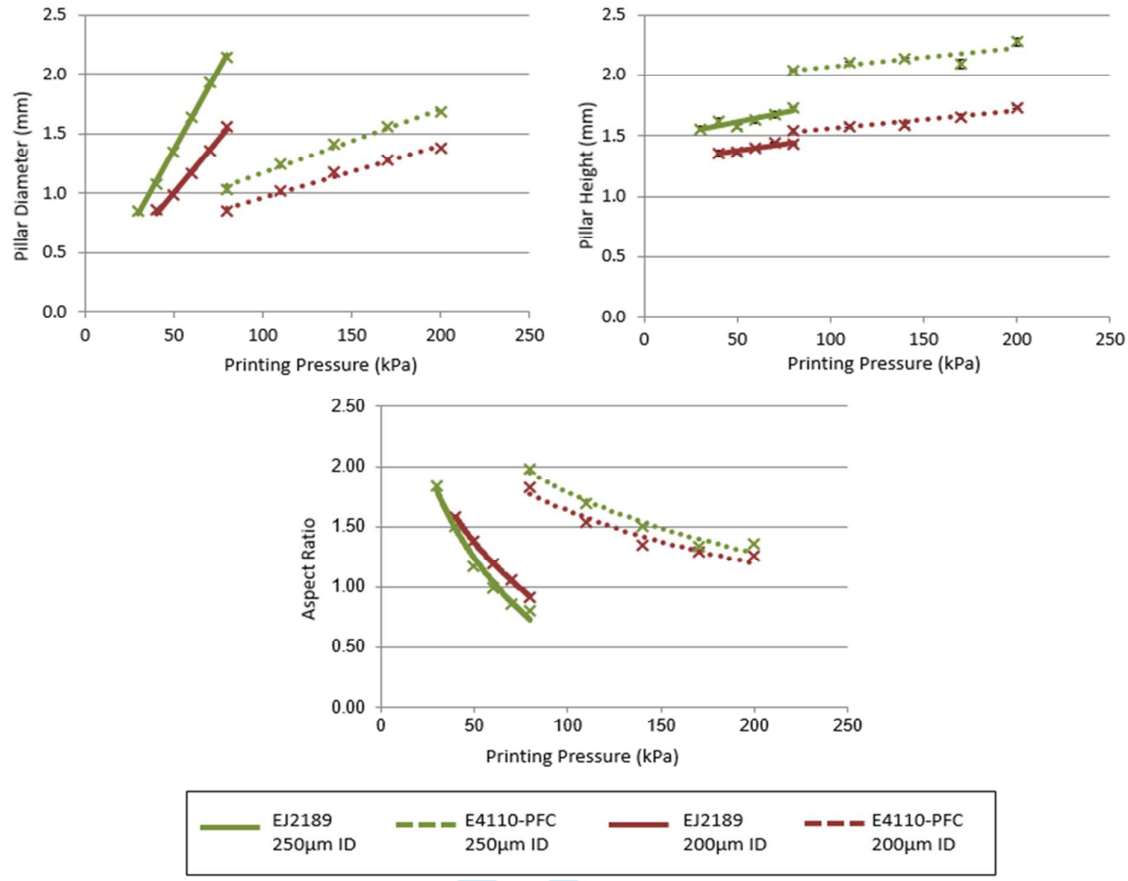

Figure 1. Diameters, height and aspect ratios of pillars produced in materials A and B using 250µm and 200µm nozzle IDs

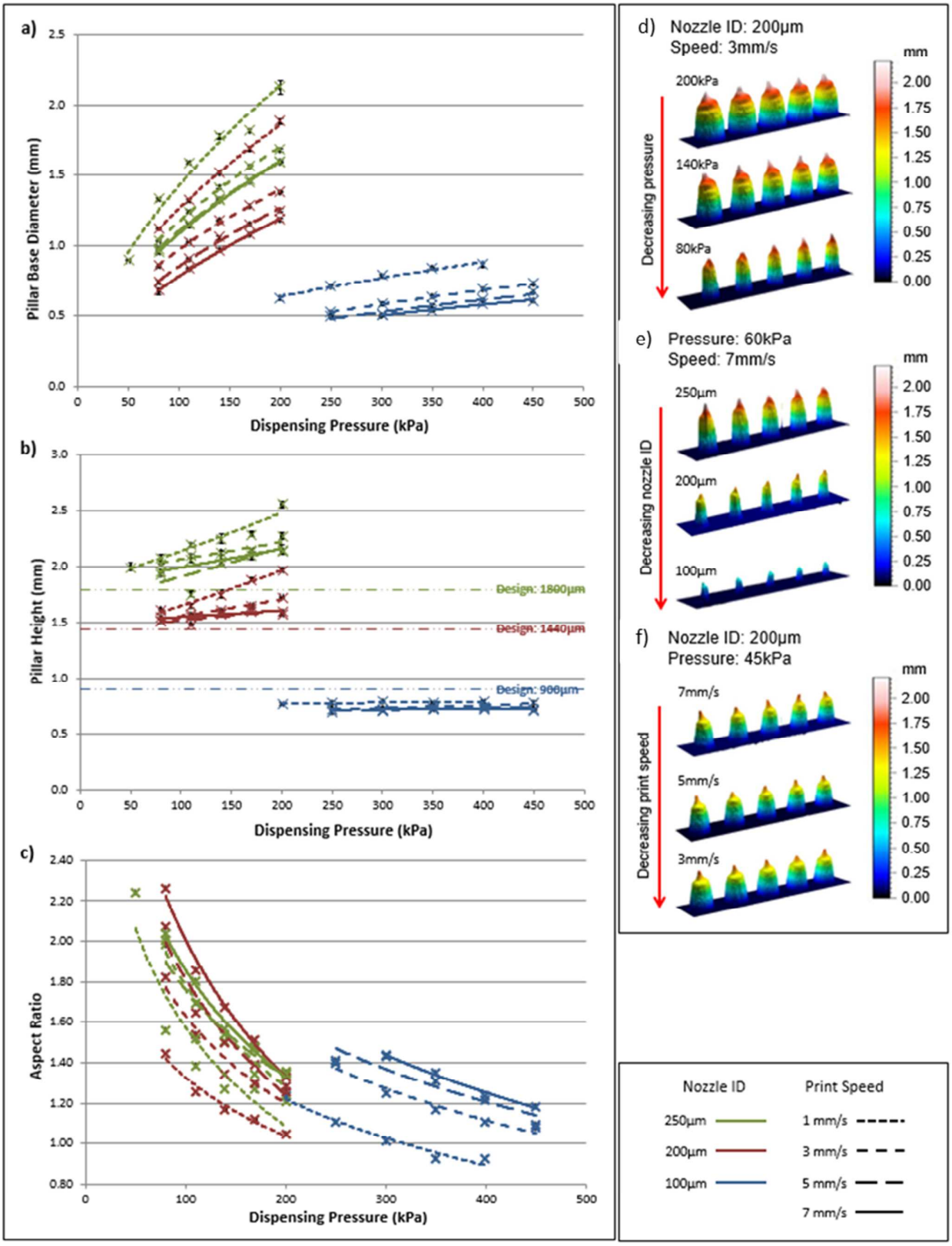

Figure 1. Graphic representation of effect of changing printing parameters on a) diameter, b) height and c) aspect ratio of profiles produced with decreasing d) pressures, e) nozzle sizes and f) print speeds

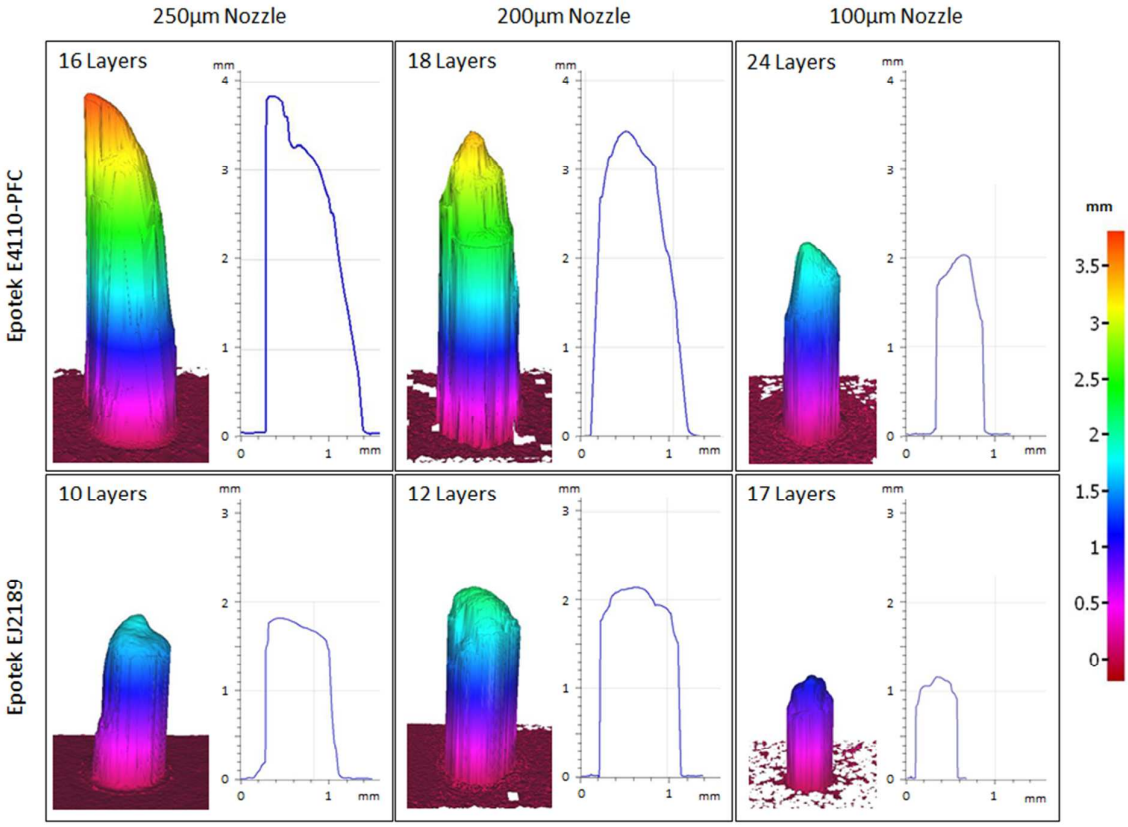

Figure 1. Comparison of largest achievable pillar structures using a combination of two materials and three nozzle sizes

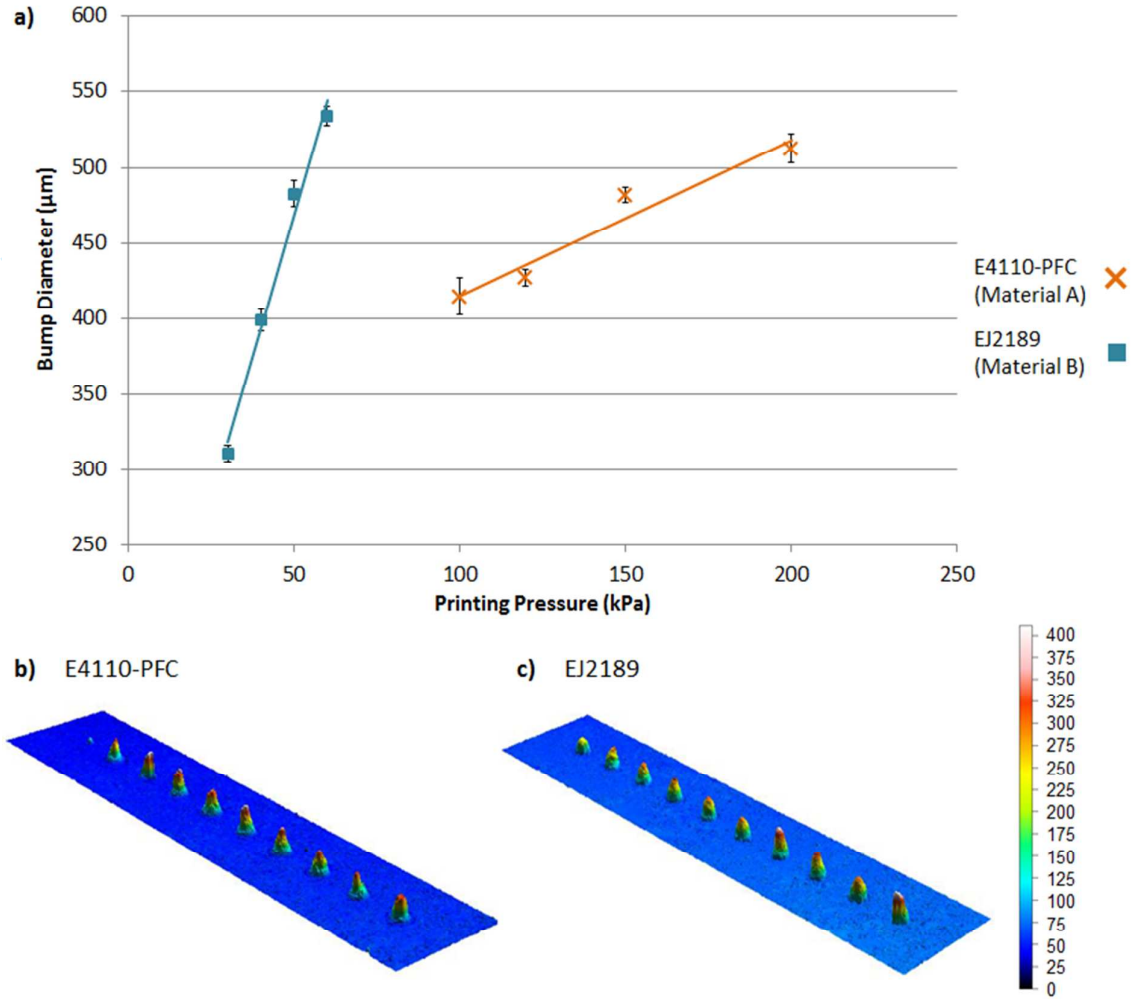

Figure 1. Comparison of interconnects printed in materials A and B

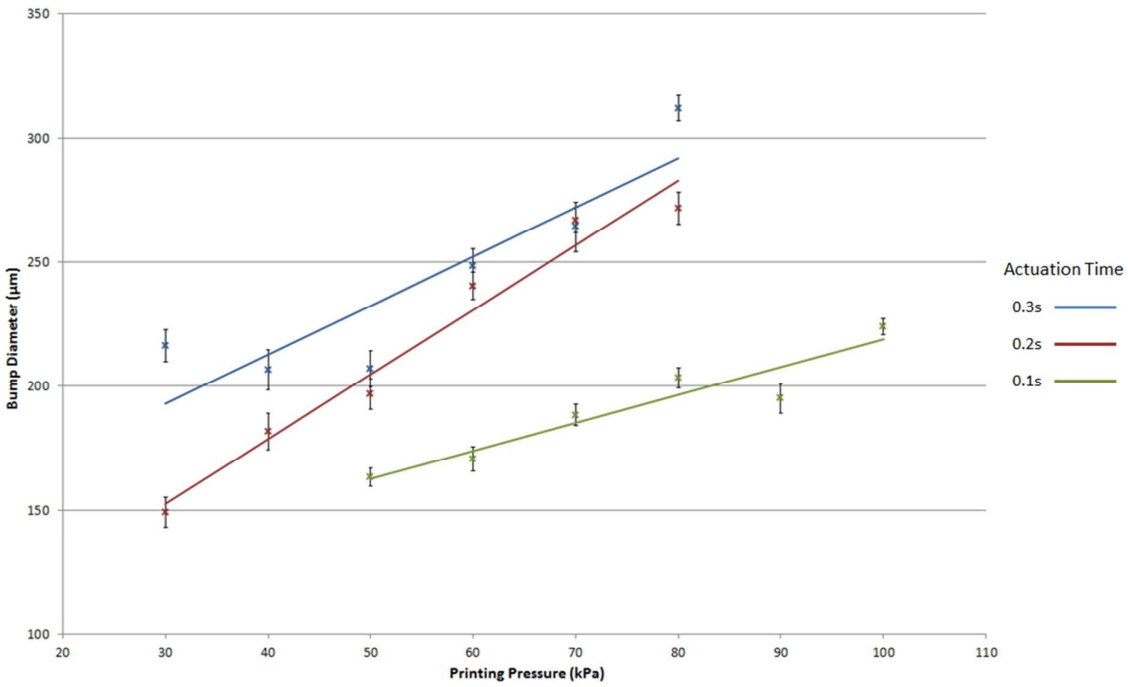

Figure 1. Relationship between printing pressure, actuation time and bump diameter at a 60µm print gap with a 100µm nozzle in material B

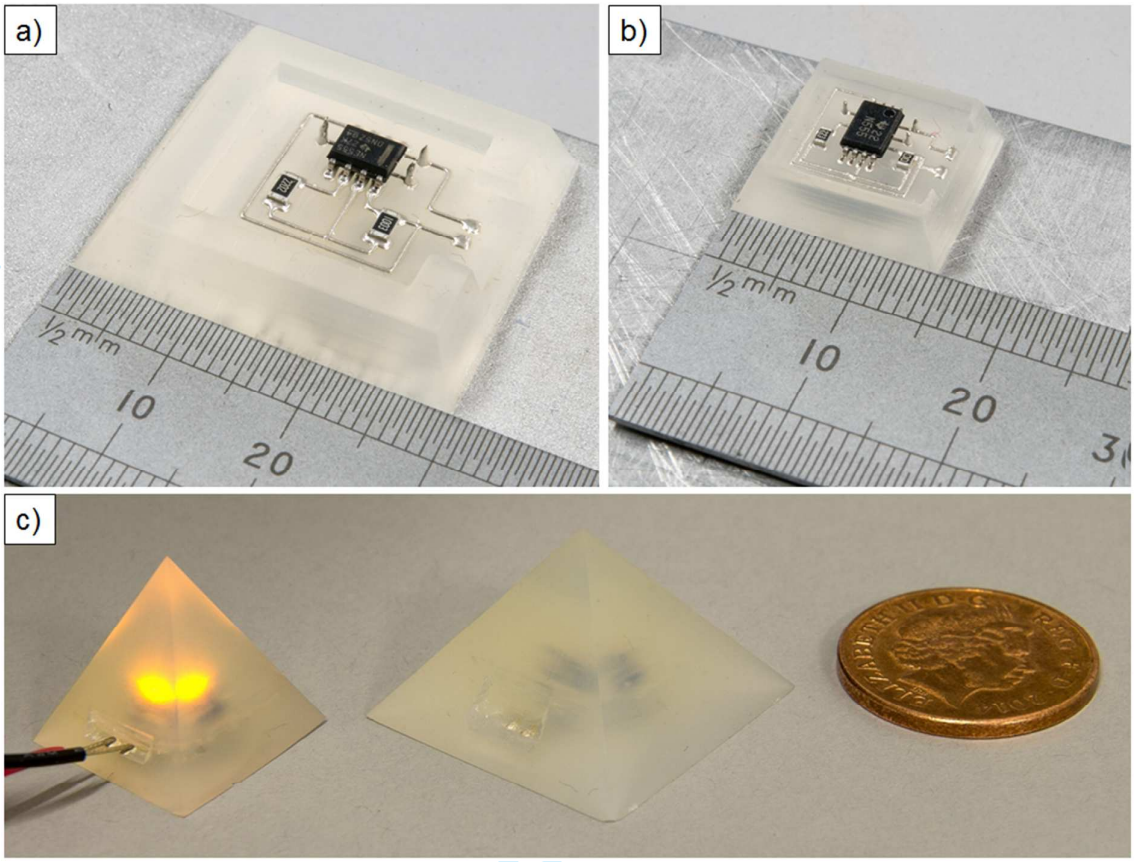

Figure 1. Comparison of demonstrator size reduction across three iterations

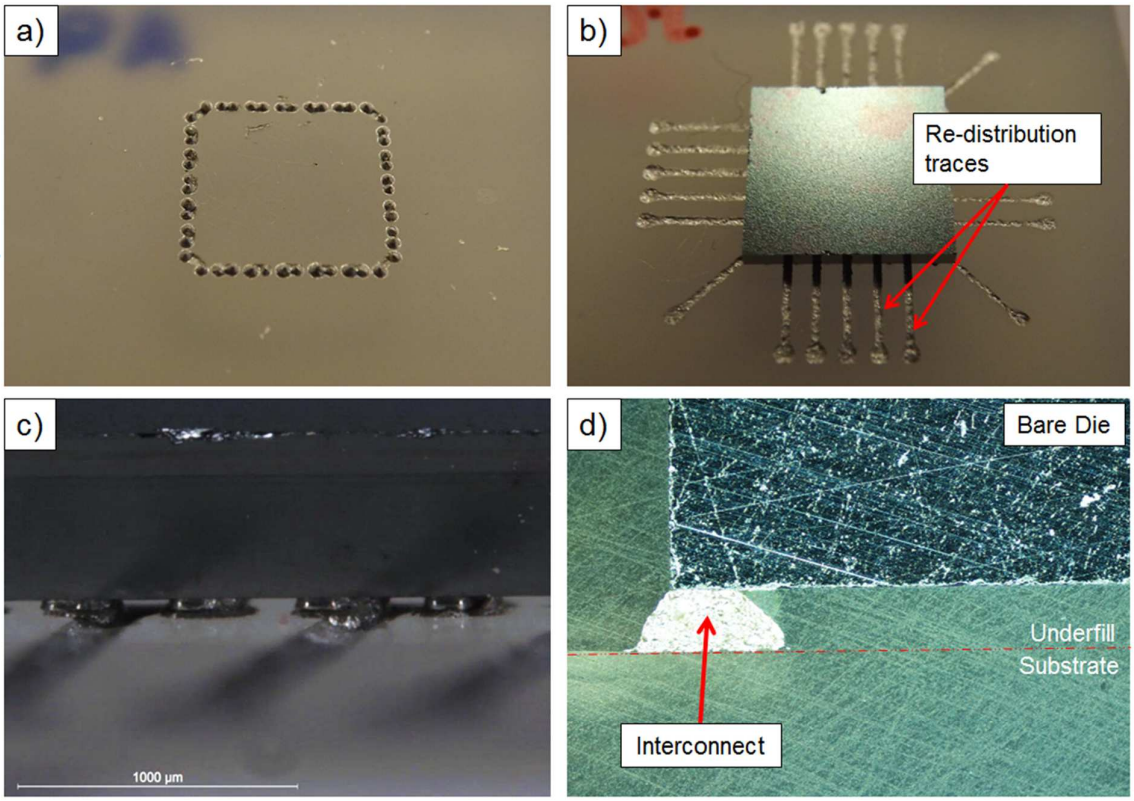

Figure 1. Stages of flip chip packaging by hybrid additive manufacturing