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UDE-based Controller Equipped with a Multi-Band-Stop Filter to Improve the Voltage Quality of Inverters

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***Abstract*—In this paper, a method to directly shape the output impedance of an inverter is proposed to reduce the total harmonic distortion of the output voltage, based on the uncertainty and disturbance estimator (UDE)-based robust control framework. It is shown that, because of the two-degree-of-freedom feature of the UDE-based control strategy, the UDE filter directly affects the inverter output impedance. A multi-band-stop filter instead of a commonly adopted low-pass filter is then proposed to directly minimize the output impedance around the harmonics to reduce the effect of nonlinear loads and assure robustness to frequency variations. Two trade-offs are revealed: one between filter bandwidth and stability and the other between robustness and the number of harmonics suppressed. The effectiveness of the proposed control strategy is fully supported by experimental results.**

***Index Terms*—Photovoltaic generators, maximum power point tracking, perturbation frequency.**

I. INTRODUCTION

INVERTERS (also known as DC-to-AC converters) play an extremely important role in sustainable energy applications such as distributed generation; hybrid, hybrid electric and more electric transportation; smart grids etc. In addition, they are widely employed in uninterruptible power supplies, home appliances (induction heaters, air conditioners, refrigerators) and variable frequency drives. In other words, inverters have become a key component of many energy-conversion-related applications.

Many research activities are being carried out on important control problems associated with inverters [1]. Minimizing the total harmonic distortion (THD) of output inverter voltage under nonlinear loads is one of the common challenges for these control problem. Deadbeat [2] and hysteresis [3] controllers as well as sliding-mode [4], observer [5] and Lyapunov function [6], [7] based approaches have been utilized to improve the voltage THD in addition to selective harmonic elimination [8], repetitive [9], harmonic voltage injection [10], model predictive [11] and offset-free robust tracking [12] control strategies. Recently, output impedance based strategies have become popular due to its influence on load sharing between several inverters operating in parallel. It was shown that output impedance of an inverter changes according to the control strategy adopted [1, 13] and may hence be reduced to enhance output voltage quality [14]. Since mainstream inverters possess low-frequency inductive output impedance, resistive [15] and capacitive [16] impedance was achieved by corresponding control methods to simplify the task of compensating load harmonics. Nevertheless, in the presence of nonlinear loads, only the values of output impedance at harmonic frequencies are of particular interest while the values at the rest of bandwidth is irrelevant for THD minimization. Multiresonant controllers were proposed to minimize the relevant output impedance [17]; however, due to the fact that fundamental frequency deviations may occur, not only the output impedance should be minimized around harmonic frequencies but also robustness to frequency deviations (note that the base frequency ω_0 deviation of $\Delta\omega_0$ becomes $n\Delta\omega_0$ around the n-th harmonic) must be assured as well.

In this paper, in order to directly influence the output impedance only at the regions of interest, dual-loop control structure is adopted [18], [19]. However, unlike typical cases [20], both loops are not decoupled due to limited available control bandwidth and therefore affect each other. Consequently, coupling effect between two loops is dealt with by considering the closed loop transfer function of the inner loop when designing the outer loop, avoiding loop decoupling constraint. It should be emphasized, that dual-loop control arrangement typically yield good performance (an interested reader is referred to [21] for detailed comparison of dual loop inverter control structures). However, PID compensators are typically utilized in multiloop control arrangements, enforced by e.g. feedforward actions, characterized by the two following drawbacks: infinite gain is achieved at DC only, calling for increased control bandwidth to reduce steady state error at non-zero frequencies and coupling between tracking and disturbance rejection due to single degree of freedom.

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Utilizing multiresonant controller as the outer loop compensator eliminates the increased control bandwidth issue but does not solve the latter drawback in addition to susceptibility to frequency deviations.

In this paper, inductor current serves as the inner loop variable compensated by a proportional controller while the outer voltage loop utilizes an Uncertainty and Disturbance Estimator (UDE) based compensator to simultaneously eliminate both above mentioned drawbacks. UDE-based control strategy is based on the assumption that a continuous signal can be approximated as it is appropriately filtered, which is true for most engineering systems [22]. It is able to quickly estimate and compensate uncertainties and disturbances, providing exceptional robust performance. The UDE-based control strategy has been further elaborated in [23] – [25] and successfully applied to several control problems [26] – [31]. The two-degree of freedom nature of UDE controllers identified in [23] is utilized in this paper to decouple the tracking and disturbance rejection of inverters. It is shown that the voltage controller may directly impose disturbance rejection through the output impedance by appropriate filter design without sensing the output current. In addition, it is revealed that while a typical UDE filter is unable to cope with the task due to limited control bandwidth, the proposed multi-band-stop-filter structure may both reduce the value of output impedance around the regions of interest and provide robustness to fundamental frequency variations. The proposed design yields several trade-offs which are discussed in detail. It should be noted that direct manipulation of inverter output impedance was recently proposed in [32] utilizing measured load current. Here, output impedance construction is carried out without any information regarding the load current.

The rest of the paper is organized as follows. The proposed control structure is presented in Section II, together with brief discussions on PWM and the current controller. The voltage controller design, based on Uncertainty and Disturbance Estimator, is proposed in Section III. Experimental validation of the proposed method is demonstrated in Section IV and conclusions are made in Section VI.

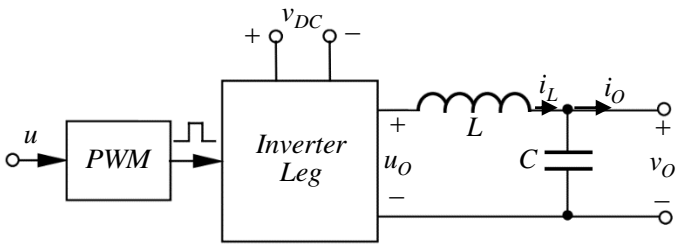


Fig. 1. A typical single-phase inverter.

II. THE PROPOSED SYSTEM

Consider a typical inverter, consisting of a single-phase LC-filter-terminated inverter leg, powered by a dc source v_{DC} and driving a nonlinear load i_O, as shown in Fig. 1. The control signal u is converted to a PWM signal to drive the inverter leg. The system may be then described by the following set of switching-period-averaged equations, with the inductor and capacitor ESRs neglected for brevity,

$$\begin{aligned} u_O(t) &= u(t-T_d)v_{DC}(t) \\ L\frac{di_L(t)}{dt} &= u_O(t)-v_O(t) \\ C\frac{dv_O(t)}{dt} &= i_L(t)-i_O(t) \end{aligned} \tag{1}$$

with T_d denoting the overall sampling and switching delay. In order to facilitate the presentation in the sequel, Table I summarizes the numerical values of system parameters.

TABLE I.
SYSTEM PARAMETER VALUES

Parameter	Value	Units
Switching frequency, T_S^{-1}	15	*kHz*
Filter inductance, L	3.4	*mH*
Filter capacitance, C	30	μF
Base frequency, ω_0	100π	*rad/s*
DC link voltage, v_{DC}	195	*V*

A. PWM sampling and switching delay

In order to minimize the overall delay T_d, asymmetric PWM has been adopted [33], where the duty cycle is updated twice in each PWM cycle, as shown in Fig. 2. The first update occurs in the beginning of the cycle, determining the ON time. The second takes place when the carrier signal reaches the maximum point, determining the OFF time. Due to the fact that PWM transport time delay depends on the duty cycle value, it should be evaluated for the worst-case possible duty-cycle [34]. In a case where the duty cycle is 100% this gives $T_{PWM} = T_S/2$ for the double-update modulation. To maximize the bandwidth of inductor current regulator, the current has to be sampled as close as possible to the PWM update instant [35] but enough to allow the DSP to perform required computations. This leads to the total delay of $T_d = T_{PWM} + T_C$, where T_C is the DSP computational time. In the proposed system, the maximum DSP computational time was found experimentally and with added margin of 10% resulted in the value of $T_C = 0.175T_S$, leading to a total transport and computation delay of $T_d = 45\mu s$.

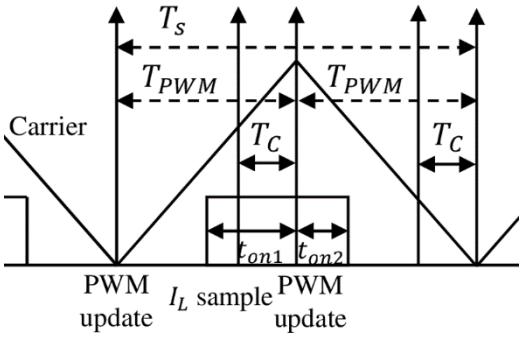


Fig 2. Switching cycle timing diagram.

B. Current controller

The inductor current can be reformulated as

$$\frac{di_L(t)}{dt} = L^{-1}\left(u(t-T_d)v_{DC}(t)-v_O(t)\right). \tag{2}$$

Modifying the control input as

$$u(t)=\frac{1}{v_{DC}(t)}\left(u'(t)+v_O(t)\right), \tag{3}$$

the current plant may be described by

$$\frac{di_L(t)}{dt}=L^{-1}\left(\frac{v_{DC}(t)}{v_{DC}(t-T_d)}\left(u'(t-T_d)+v_O(t-T_d)\right)-v_O(t)\right) \tag{4}$$
$$\approx L^{-1}u'(t-T_d),$$

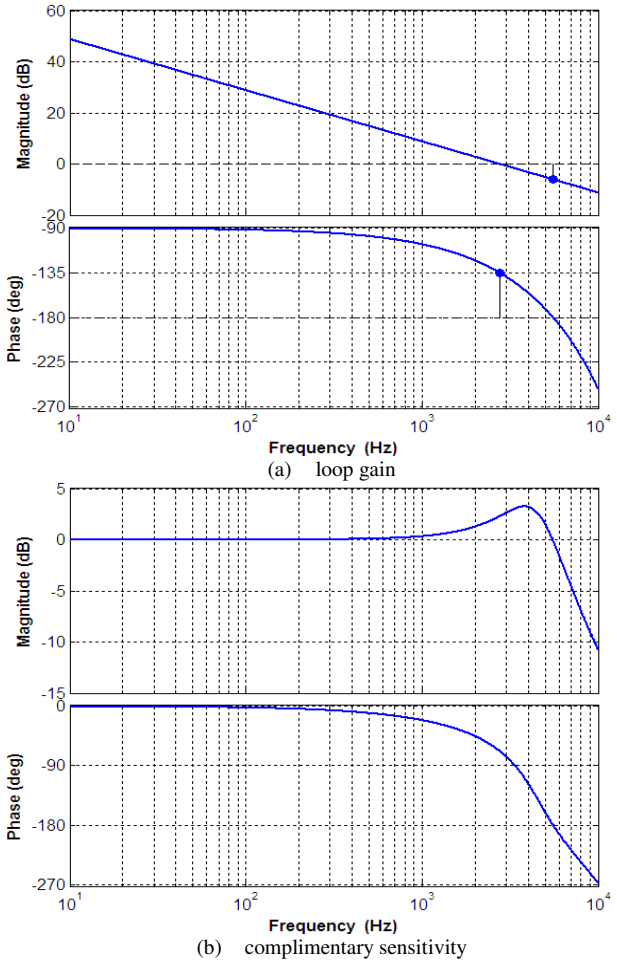
as T_d^{-1} is much higher than bandwidths of v_{DC} and v_O. Since the modified plant is nearly disturbance-free, proportional controller

$$u'(t)=K_{PI}\left(i_L^*(t)-i_L(t)\right) \tag{5}$$

with $i_L^*(t)$ denoting inductor current reference signal, is selected. Current loop gain and complementary sensitivity function are then obtained as

$$L_I(s)=\frac{K_{PI}L^{-1}}{s}e^{-T_d s} \tag{6}$$

and



(a) loop gain

(b) complimentary sensitivity

Fig. 3. Current loop performance merits for K_{PI} = 59 and T_d = 45μs.

$$T_I(s)=\frac{L_I(s)}{1+L_I(s)}=\frac{K_{PI}L^{-1}}{se^{T_d s}+K_{PI}L^{-1}}, \tag{7}$$

respectively. Selecting K_{PI} = 59 leads to current loop bandwidth of 2762Hz with 45° phase margin and 6dB gain margin, as shown in Fig. 3a. Fig. 3b gives the Bode diagram of the complementary sensitivity function, which is of extreme importance for voltage controller design, since $T_I(s)$ serves as voltage loop actuator.

C. Voltage controller

Note that i_L^* rather than i_L is set by the voltage controller, i.e. the current closed loop controller $T_I(s)$ must be properly taken into account. Output voltage dynamics may be rewritten as

$$\frac{dv_O(t)}{dt}=C^{-1}\left(i_L(t)-i_O(t)\right)$$
$$=\left(C_n^{-1}+\Delta C^{-1}\right)\left(i_L^*(t)+\Delta i_L(t)-i_O(t)\right)=C_n^{-1}\left(i_L^*(t)-i_O^d(t)\right), \tag{8a}$$

where C_n and ΔC respectively denote nominal and uncertain parts of C, $i_L = i_L^* + \Delta i_L$ with Δi_L representing inductor current tracking error and

$$i_O^d(t)=-C_n\Delta C^{-1}i_L^*(t)-\left(1+C_n\Delta C^{-1}\right)\left(\Delta i_L(t)-i_O(t)\right) \tag{8b}$$

expresses the total lumped uncertainty and disturbance current.

Define the desired closed-loop behavior of v_O by the output of a linear time-invariant stable reference model

$$\dot{v}_{OR}(t)=-\omega_R v_{OR}(t)+\omega_R v_O^*(t) \tag{9}$$

with v_O^* denoting the output voltage reference signal and ω_R > 0. The controller goal is to drive the error between the reference model and inverter outputs

$$e_O(t)=v_{OR}(t)-v_O(t) \tag{10a}$$

to zero by forcing the following stable error dynamics,

$$\frac{de_O(t)}{dt}=-\omega_R e_O(t). \tag{10b}$$

Combining (8) - (10) results in

$$i_L^*(t)=K_{PV}\left(v_O^*(t)-v_O(t)\right)+i_O^d(t) \tag{11}$$

with $K_{PV} = C_n\cdot\omega_R$. The control action (11) cannot be applied directly since i_O^d is unknown. This problem is dealt with as follows. Note that according to (8a),

$$i_O^d(t)=i_L^*(t)-C_n\frac{dv_O(t)}{dt} \tag{12}$$

Obviously, (12) cannot be substituted in (11) as is. A UDE-based approach replaces i_O^d in (11) with its filtered estimate, given by

$$\hat{i}_O^d(t)=i_O^d(t)*g(t)=\left(i_L^*(t)-C_n\frac{dv_O(t)}{dt}\right)*g(t), \tag{13}$$

where $g(t)$ is the impulse response of a frequency-selective linear time-invariant filter $G(s)$ and '*' is the convolution operator. The control law is then derived as (cf. Fig. 4)

$$i_L^*(t)=i_{L0}^*(t)+\tilde{i}_O^d(t)$$
$$=K_{PV}\left(v_O^*(t)-v_O(t)\right)+\left(i_L^*(t)-C_n\frac{dv_O(t)}{dt}\right)*g(t). \tag{14}$$

It is interesting to note that the voltage controller structure resembles that of a classical disturbance observer (DOB) [36] based compensator, consisting of nominal controller (here, K_{PV}) and disturbance observer (here, *UDE*). Therefore, even though proportional nominal controller is used in the subsequent derivations to shape the tracking response, a more advanced compensator (e.g. PID, PR etc) may in general replace K_{PV}.

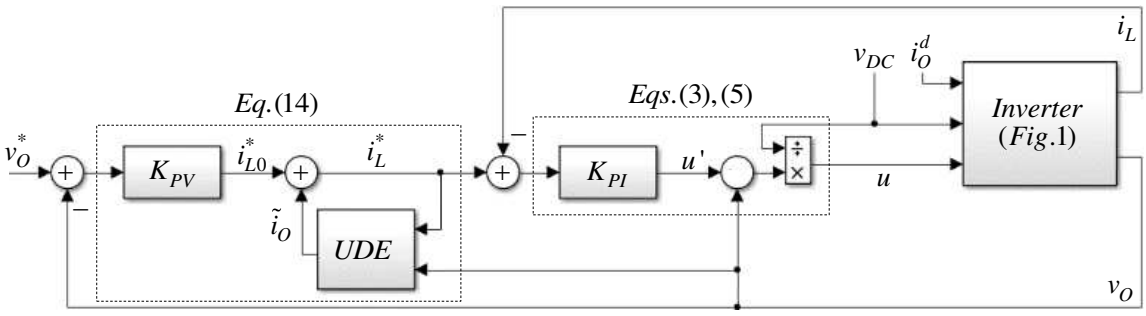


Fig. 4. The proposed control structure.

Taking Laplace transform of (14) and rearranging, there is

$$I_L^*(s) = C_n\left(\underbrace{\frac{\omega_R}{1-G(s)}}_{H_{FF}(s)} V_O^*(s) - \underbrace{\frac{\omega_R + sG(s)}{1-G(s)}}_{H_{FB}(s)} V_O(s)\right). \tag{15}$$

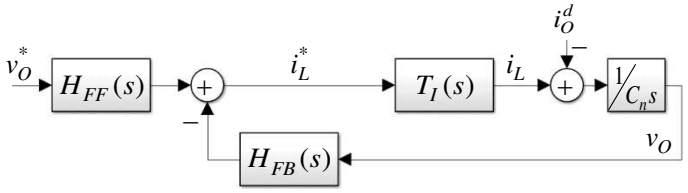


Fig. 5. Equivalent voltage loop diagram.

The overall voltage loop structure is shown in Fig. 5 with $T_I(s)$ playing the actuator role. Corresponding loop gain is then

$$L_V(s) = \frac{\omega_R + sG(s)}{s\left(1-G(s)\right)} T_I(s), \tag{16}$$

indicating infinite gain at DC and frequencies associated with the roots of $1–G(s)$. Substituting (15) into (8) and rearranging results in the following closed-loop dynamics,

$$V_O(s) = \underbrace{\frac{H_{FF}(s)T_I(s)}{s + H_{FB}(s)T_I(s)}}_{T_V(s)} V_{OR}(s) - \underbrace{\frac{C_n^{-1}}{s + H_{FB}(s)T_I(s)}}_{Z_O(s)} I_O^d(s). \tag{17}$$

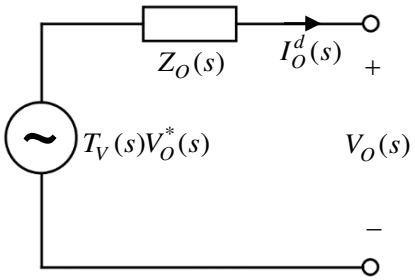


Fig. 6. Equivalent model of the single-phase inverter.

The inverter under the proposed closed loop control can then be modeled as a series connection of voltage source $T_V(s)V_O^*(s)$ and an output impedance $Z_O(s)$, as shown in Fig. 6, taking the voltage $V_O(s)$ as the output voltage and the current $I_O^d(s)$ as the output current. Obviously, it is expected that $T_V(s)\rightarrow 1$ in order to achieve good tracking performance and $Z_O(s)\rightarrow 0$ in order to achieve good disturbance rejection at relevant frequencies. For the case of tracking problem, assume the total uncertainty and disturbance current and output voltage reference are given by

$$i_O^d(t) = \sum_{n=1}^{\infty} I_n \sin(n\omega_0 t + \phi_n) \tag{18}$$

and

$$v_O^*(t) = V_M^* \sin\omega_0 t, \tag{19}$$

respectively. Then, there is

$$\begin{aligned} & v_O(t) \\ & = V_M^* \sin\omega_0 t - \sum_{n=1}^{\infty} I_n \left|Z_O(n\omega_0)\right| \sin(n\omega_0 t + \phi_n + \arg Z_O(n\omega_0)) \\ & = v_{O1}(t) + v_{OH}(t), \end{aligned} \tag{20}$$

where

$$\begin{aligned} v_{O1}(t) &= V_M^* \sin\left(\omega_0 t\right) - I_1 \left|Z_O(\omega_0)\right| \sin(\omega_0 t + \phi_1 + \arg Z_O(\omega_0)) \\ &= V_1 \sin\left(\omega_0 t + \theta\right) \end{aligned} \tag{21}$$

with

$$V_1 = \sqrt{\left(V_M^*\right)^2 + \left(I_1\left|Z_O(\omega_0)\right|\right)^2 - 2V_M^* I_1 \left|Z_O(\omega_0)\right| \cos\left(\phi_1 + \arg Z_O(\omega_0)\right)}$$

$$\theta = tg^{-1} \frac{\omega_0 \left|Z_O(\omega_0)\right| \sin\left(\phi_1 + \arg Z_O(\omega_0)\right)}{I_1 \left|Z_O(\omega_0)\right| \cos\left(\phi_1 + \arg Z_O(\omega_0)\right) - V_M^*};$$

and

$$v_{OH}(t) = -\sum_{n=2}^{\infty} I_n \left|Z_O(jn\omega_0)\right| \sin(n\omega_0 t + \phi_n + \arg Z_O(jn\omega_0)). \tag{22}$$

It should be emphasized that v_{O1} and v_{OH} are orthogonal and hence decoupled. As is well known, the quality of the output voltage is typically quantified by the total harmonic distortion (THD) defined as

$$THD_V = \frac{\sqrt{\sum_{n=2}^{\infty} \left(I_n \left|Z_O(jn\omega_0)\right|\right)^2}}{V_1}. \tag{23}$$

Obviously, it is mainly influenced by the magnitude of output impedance at harmonic frequencies (typically odd multiples of base frequency in single phase systems and $6n\pm1$ in three-phase applications). Hence, it is desirable to reduce the latter as much as possible in order to minimize THD_V. Nevertheless, observing (21) reveals that even if THD_V is minimized, v_O and v_O^* may still differ due to the voltage drop on the output

impedance at base frequency $|Z_O(\omega_0)|$. Consequently, it is desirable to reduce $|Z_O(n\omega_0)|$ for $n = 1\ldots N$ with N denoting the order of the highest load harmonic possessing significant energy.

III. Design of UDE-based voltage controller

In case $T_I(s) = 1$, (17) reduces to

$$V_O(s) = \underbrace{\frac{\omega_R}{s+\omega_R}}_{T_V(s)} V_{OR}(s) - \underbrace{\frac{C_n^{-1}}{s+\omega_R}\left(1-G(s)\right)}_{Z_O(s)} I_O^d(s). \qquad (24)$$

Hence, voltage loop complementary sensitivity function $T_V(s)$ follows that of reference model (8) while tracking is decoupled from disturbance rejection by $G(s)$, as expected from [23]. In addition, output impedance $Z_O(s)$ is formed by series connection of two frequency-selective filters: $Z_{O1}(s) = C_n^{-1}(s+\omega_R)^{-1}$ and $Z_{O2}(s) = 1-G(s)$. This means the output impedance can be designed by selecting a suitable UDE-filter $G(s)$. Apparently, in case $C_n^{-1} > \omega_R$, the magnitude of $Z_{O1}(s)$ is greater than 0dB for frequencies below $\omega = \sqrt{C_n^{-2} - \omega_R^2}$. Therefore, in order to reduce the output impedance, ω_R should be increased as much as possible (this would also improve tracking). Alternatively, output impedance may be reduced by imposing $Z_{O2}(s)$ as close to zero as possible at relevant frequencies. Unfortunately, since $T_I(s)$ serves as the voltage loop actuator, available control bandwidth for given stability margins is limited. Therefore, tracking – disturbance rejection trade-off is expected to appear. The design is then carried out as follows. First, minimum tracking bandwidth $\omega_{R,MIN}$ is set. Then, $G(s)$ is selected to minimize the magnitude of $Z_O(s)$ while respecting minimum allowed stability margins. In the subsequent analysis, $\omega_{R,MIN} = 10\cdot\omega_0$ is designated to assure decent tracking and minimum stability margins are set to 45° and 6dB, respectively.

A. Maximizing tracking bandwidth

As mentioned above, two-degrees-of-freedom control structures possess tracking/disturbance rejection trade-off. In case disturbance rejection is compromised, tracking may be enhanced. It is therefore possible to maximize the tracking bandwidth by setting $G(s) = 0$. The loop gain is then given by

$$L_V(s) = \frac{\omega_R}{s}\frac{K_{PI}L^{-1}}{se^{T_d s} + K_{PI}L^{-1}} \qquad (25)$$

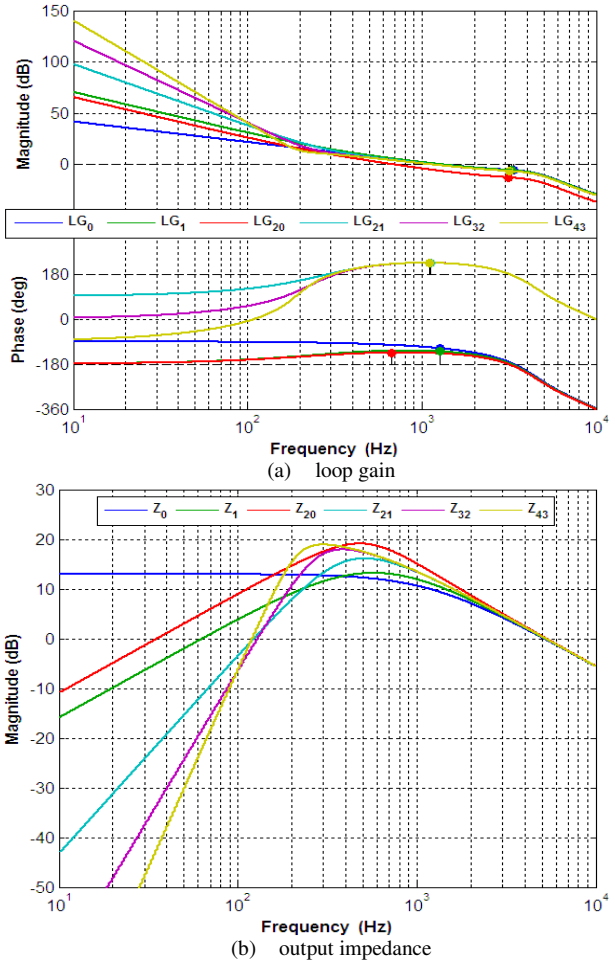
and hence $\omega_R = \omega_{R,MAX} = 2\pi\cdot 1196$ rad/s may be achieved, bringing the system to the 6dB gain margin limit, as shown in Fig. 7a. Unfortunately, the resulting output impedance magnitude would be higher than 0dB for frequencies below $2\pi\cdot 5170$ rad/s (cf. Fig. 7b), i.e. all the significant base frequency multiples harmonics of the load current will be amplified.

B. Typical UDE filters based design

Most of the applications employing UDE-based controllers utilize first order low pass Butterworth filters. Nevertheless, as stated in [23], [37] increasing filter order/decreasing relative degree/increasing cutoff frequency improve disturbance rejection. Unfortunately, it is further shown than under bandwidth constraints, trade-off exists between the three. The consequences of utilizing different low pass Butterworth filters as UDE filters were investigated by applying the filters summarized in Table II (only strictly proper filters were considered in order to assure implementability of $sG(s)$ in (15)).

TABLE II.
LOW PASS BUTTERWORTH FILTERS

order	$\omega_R/2\pi$	$\omega_F/2\pi$	$G(s)$
0	1196	0	0
1	500	664	$\frac{\omega_F}{s+\omega_F}$
20	500	530	$\frac{\omega_F^2}{s^2+1.41\omega_F\cdot s+\omega_F^2}$
21	500	393	$\frac{1.41\omega_F s+\omega_F^2}{s^2+1.41\omega_F s+\omega_F^2}$
32	500	279	$\frac{2\omega_F s^2+2\omega_F^2 s+\omega_F^3}{s^3+2\omega_F s^2+2\omega_F^2 s+\omega_F^3}$
43	500	215	$\frac{2.61\omega_F s^3+3.41\omega_F^2 s^2+2.61\omega_F^3 s+\omega_F^4}{s^4+2.61\omega_F s^3+3.41\omega_F^2 s^2+2.61\omega_F^3 s+\omega_F^4}$



(a) loop gain

(b) output impedance

Fig. 7. Voltage loop performance merits utilizing filters of Table II.

The tracking bandwidth was set to $\omega_{R,MIN}$ and then filter cutoff frequency satisfying the above-set minimum stability margins was determined. Figs. 7a and 7b demonstrate corresponding loop gains (LG) and output impedances, respectively. Two important conclusions may be then drawn:

- Even though the cutoff frequency of the filter $G_{20}(s)$ is higher than that of $G_{21}(s)$, disturbance rejection capabilities of the latter are better, i.e. decreasing relative degree increases disturbance rejection. Hence, only filters with relative degree of one were considered further.
- Increasing filter order forces reducing the cut-off frequency yet improves low-frequency disturbance rejection (see the value of output impedance magnitude at base frequency). Unfortunately, medium-frequency disturbance rejection is deteriorated (the values of output impedance magnitude at [100Hz, 2000Hz] frequency range are higher than 0dB). Consequently, increasing filter order does not necessarily reduce THD, which eventually depends on the harmonic content of load current.

To conclude, utilizing low pass UDE filters under given bandwidth restrictions is insufficient to reduce the output impedance below 0dB at frequency range where load current is expected to possess significant energy.

C. Shaping of the output impedance

Note that $Z_{O2}(s)$ rather than $G(s)$ directly affects the output impedance. Therefore, it is suggested to select $Z_{O2}(s)$ and then derive the UDE filter as $G(s) = 1 - Z_{O2}(s)$. Since output impedance minimization is required only at base frequency multiples, it is proposed to construct $Z_{O2}(s)$ as a bank of series connected band-stop filters,

$$Z_{O2}(s) = \prod_{n=1}^{N} H_n(s), \tag{26}$$

where n-th harmonic filter stop band is is given by $[n\cdot\omega_0\cdot k, n\cdot\omega_0/k]$ with $k < 1$, of which the ideal shape is shown in Fig. 8. Obviously, in order to increase filter robustness to fundamental frequency variations, the bandwidth of each filter should be maximized, i.e. k should be chosen as small as possible. Unfortunately, it is impossible to freely increase the overall stop band of $Z_{O2}(s)$ without violating the minimum stability margins due to limited available control bandwidth. Consequently, maximum attainable stop band is shared by n filters, i.e. trade-off exists between the number of series connected filters (N) and the bandwidth of each filter (k).

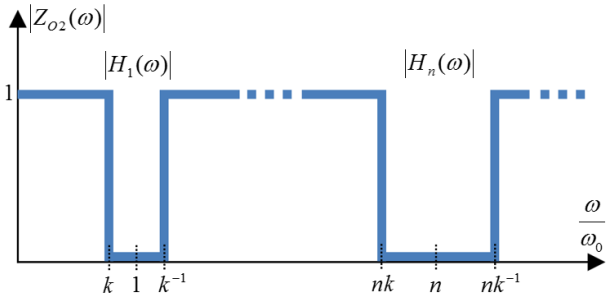
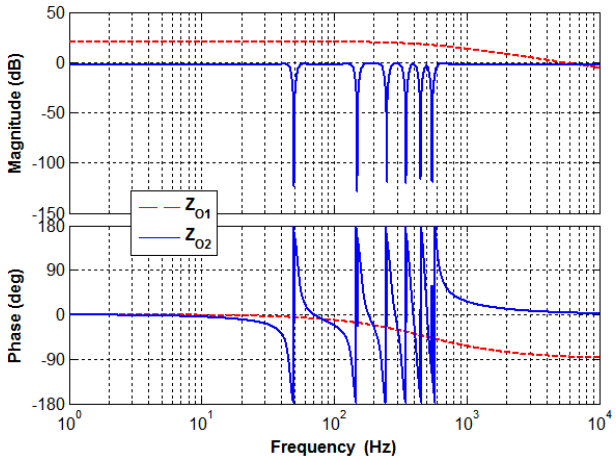
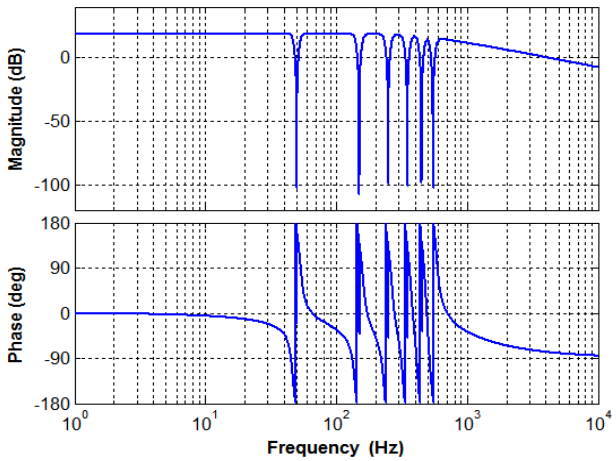


Fig. 8. Ideally desired magnitude of $Z_{O2}(s)$.

In this work, elliptic band-stop filters were employed due to their ability to attain a given transition width with the smallest order [38]. $Z_{O2}(s)$ was constructed by series connection of 6 second-order filters (n = 1,3,5,7,9,11) with pass-band and stop-band ripples of 0.35dB and 60dB, respectively. In order to comply with minimum stability margins, the smallest attainable value of k was found to be 0.89. The magnitude response of designed $Z_{O2}(s)$ is shown in Fig. 9a together with that of $Z_{O1}(s) = C_n^{-1}(s+\omega_{R,MIN})^{-1}$ and the resulting output impedance is depicted in Fig. 9b. It is interesting to note that $Z_O(s)$ is resistive at harmonic frequencies. Since the magnitude Z_{O1} remains around 20dB throughout the region of interest, the worst-case magnitude of the impedance around harmonic frequencies is -40dB, as shown in Fig. 10.



(a) $Z_{O1}(s)$ and $Z_{O2}(s)$.



(b) $Z_O(s) = Z_{O1}(s)\cdot Z_{O2}(s)$.

Fig. 9. Output impedance and its components.

Note that compared to the $G(s) = 0$ case, the magnitude of output impedance is above 0dB for all but six relevant frequencies below $2\pi\cdot5170$ rad/s. Nevertheless, values of output impedance magnitude at frequencies other than in the vicinity of harmonic frequencies are not important. Hence, any harmonic load is expected to be well rejected by the inverter. Moreover, it is apparent that the magnitude of the impedance remains below -10dB in case the base frequency deviates $\pm$1Hz around its nominal value, demonstrating the robustness. Bode plot of the corresponding UDE filter $G(s) = 1 - Z_{O2}(s)$ is shown in Fig. 11. It is important to emphasize that the latter possesses unity magnitude and zero phase at the first six base frequency multiples, as desired. Fig. 12 demonstrates the resulting loop gain. It is interesting to note that the gain margin of ~6dB is the limiting factor and not the phase margin (~65°).

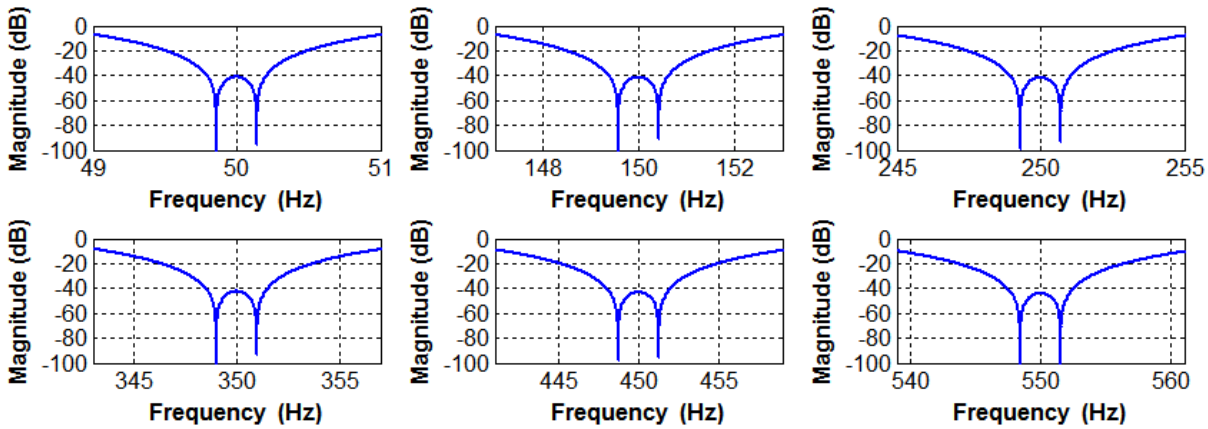


Fig. 10. Output impedance zoomed around harmonic frequencies.

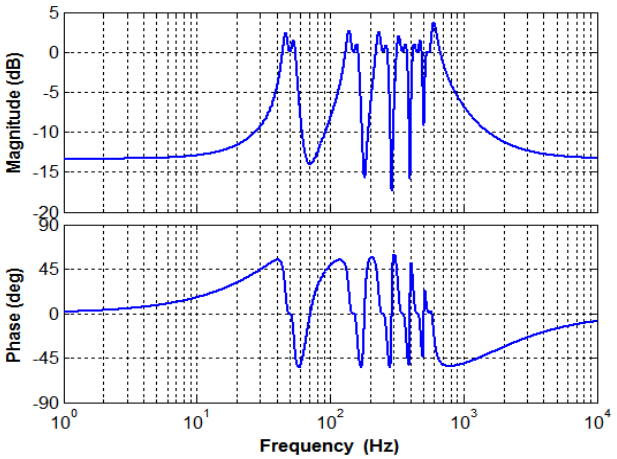


Fig. 11. Bode plot of the designed UDE filter $G(s) = 1 - Z_{O2}(s)$.

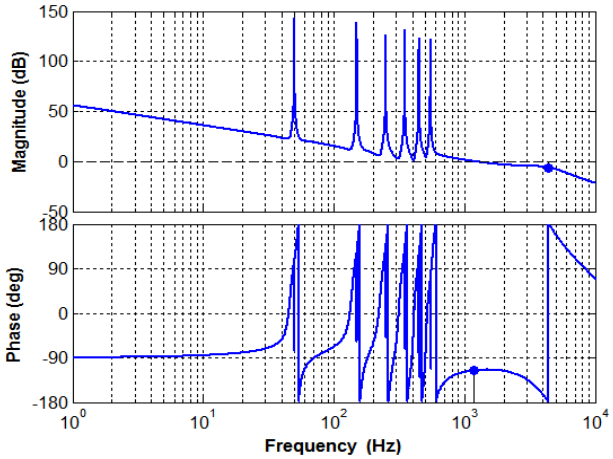


Fig. 12. The resulting voltage loop gain.

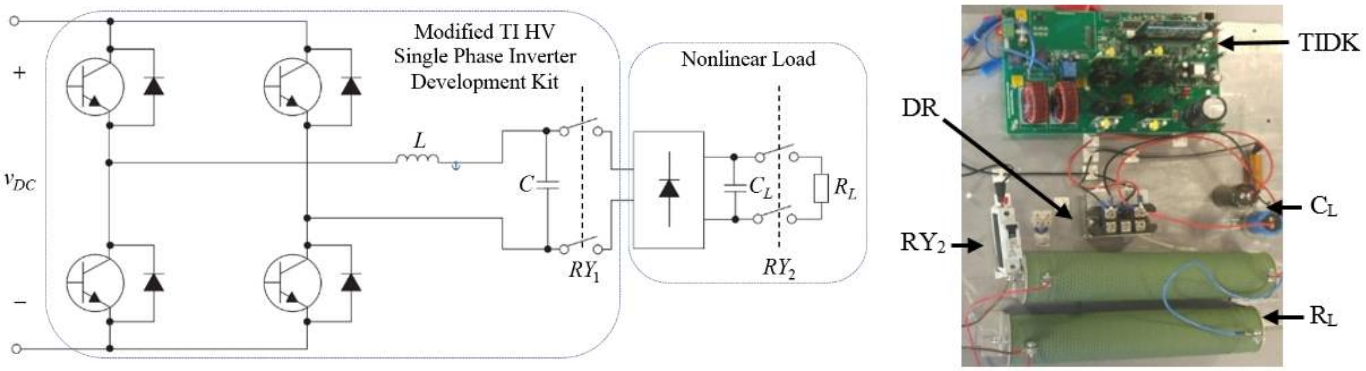
IV. Experimental Verification

In order to validate the proposed control system, modified Texas Instruments High Voltage Single Phase Inverter Development Kit (TIDK) was utilized. The inverter was initially loaded by a 33Ω resistor to establish a baseline; then, the resistor was replaced by a diode rectifier (DR) with heavy RC load, as shown in Fig. 13a. Corresponding nonlinear load parameter values summarized in Table III. Inverter parameters of the experimental setup match the values given in Table I. The control system was implemented digitally using Concerto F28M35 control card. The setup is pictured in Fig. 13b.

TABLE III.
NONLINEAR LOAD PARAMETER VALUES

Parameter	Value	Units
Load resistance, R_L	50	Ω
Load capacitance, C_L	940	μF

In the first experiment, current loop performance was examined by verifying the step response under short-circuit conditions. The result is shown in Fig. 14. According to the target current loop bandwidth of 2762Hz, 288μs is the expected five-time-constants transient duration, which is well verified.



(a) Schematics.

(b) Pictured.

Fig. 13. Experimental hardware with nonlinear load connected.

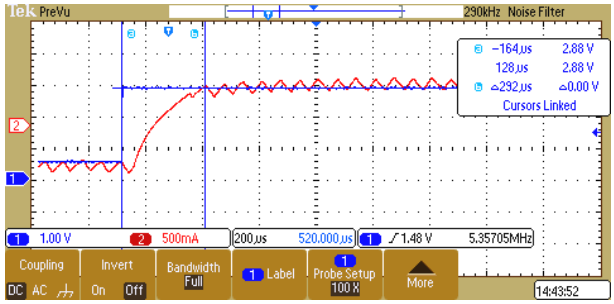
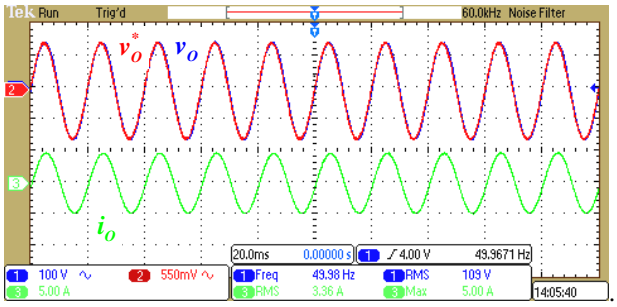
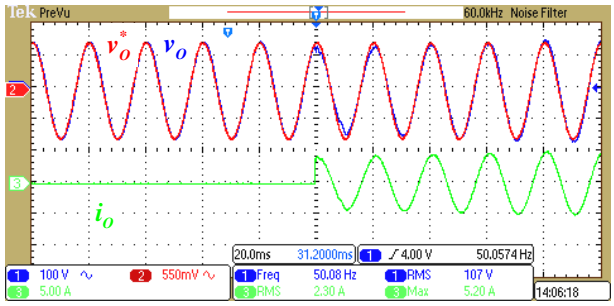


Fig. 14. Experimental results: Current-loop step response.

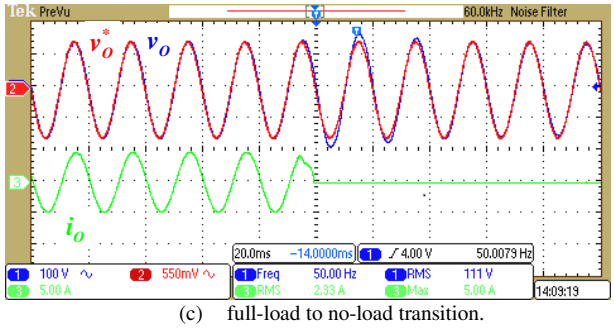
In the second experiment, nominal base frequency system operation was validated under both linear and nonlinear loads. Output voltage reference signal was set to (19) with $V_M^* = 110\sqrt{2}$V. Steady state, operation, no-load to full-load and full-load to no-load transitions are depicted in Figs. 15 and 16 for linear and nonlinear loads, respectively.



(a) steady state.



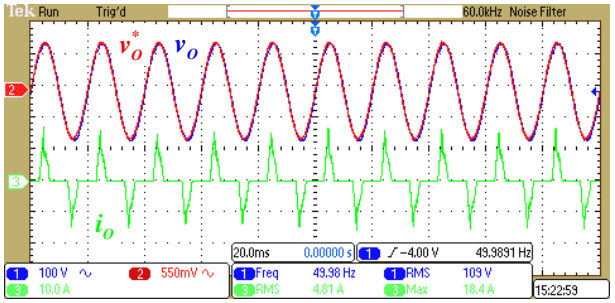
(b) no-load to full-load transition.



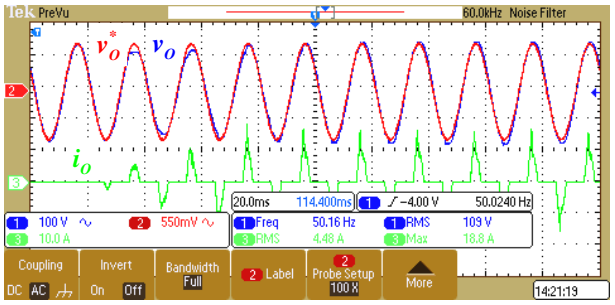
(c) full-load to no-load transition.

Fig. 15. Experimental results: Operation under linear load, nominal base frequency.

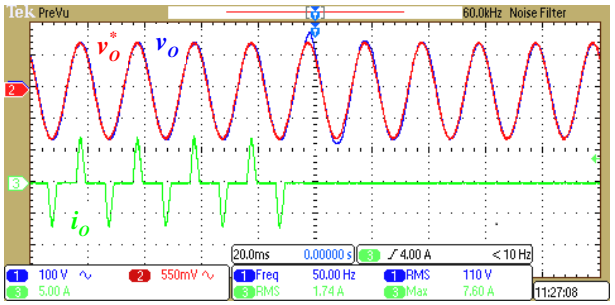
It may be concluded that the system operates well under both types of load in steady state. Fig. 17 demonstrates respective experimental frequency domain distributions and total harmonic distortions of the output voltage. The linear load case THD_V = 0.87% may actually serve as a baseline, defining the noise floor. Observing the results of operation under nonlinear load, while taking the baseline into account, it may be concluded that voltage harmonics up to 11th are nearly absent, as planned. Corresponding experimental THD_V was obtained as 2.05%, validating excellent control algorithm performance.



(a) steady state.



(b) no-load to full-load transition.

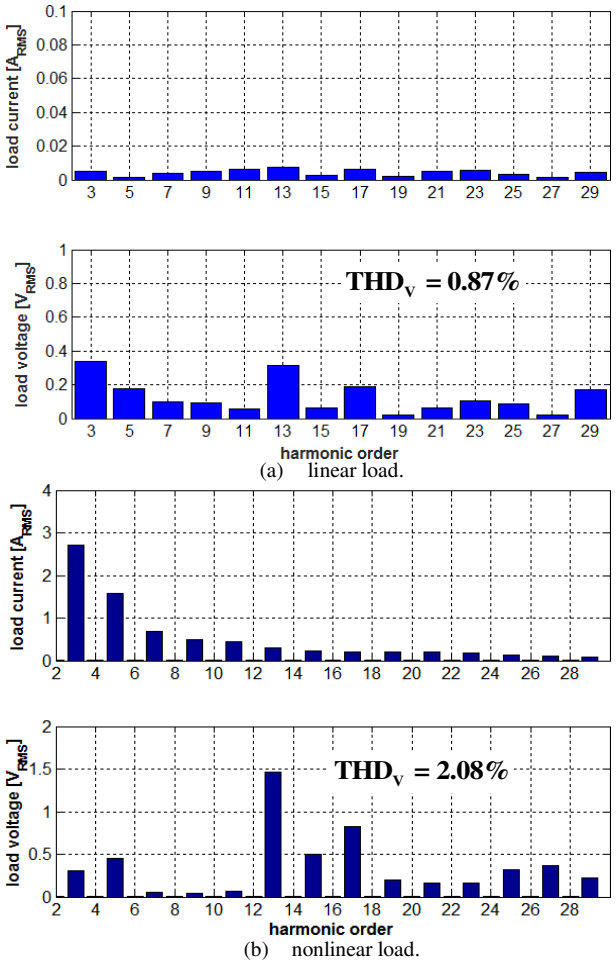


(c) full-load to no-load transition.

Fig. 16. Experimental results: Operation under nonlinear load, nominal base frequency.

On the other hand, it takes around one cycle for the system to settle in both cases. This transient performance is satisfactory but might not be optimal due to the relatively large convergence time of the multi-band-stop-filter utilized. This is the price to pay for the excellent steady state performance.

For the sake of comparison, the system was also tested under nonlinear loading employing typical UDE controller with first and third order low pass Butterworth filters (cf. Table II). Corresponding frequency domain distributions (time-domain results are omitted for brevity) and THD_V values are depicted in Fig. 18 and compared to steady state operation with the multi-band-stop filter. Apparently, UDE controller equipped with the proposed filter outperforms the classical one for both low pass filter types.



(a) linear load.

(b) nonlinear load.

Fig. 17. Experimental results: Spectra of output voltage and current.

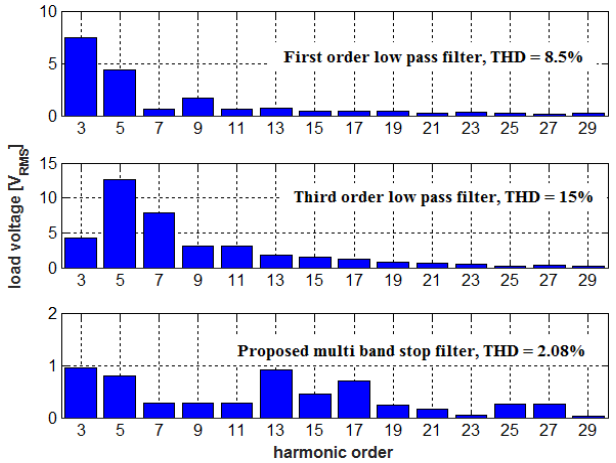
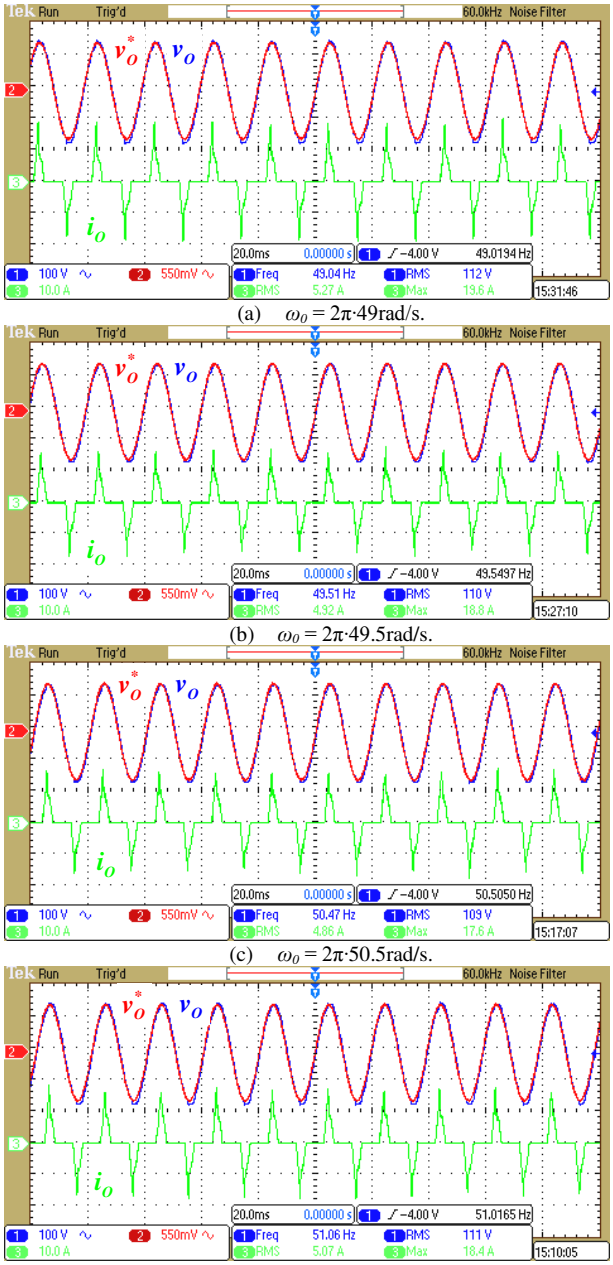


Fig. 18. Output voltage spectra comparison for different filter types.

In the last experiment, steady-state operation of nonlinearly loaded system was inspected under fundamental frequency deviation up to ±1Hz to verify the robustness. Experimental results are shown in Fig. 19 with corresponding values of THD_V summarized in Fig. 20 along with their corresponding simulated values. Apparently, THD_V remains low despite base frequency variations and is in good agreement with simulations.



(a) $\omega_0 = 2\pi \cdot 49$rad/s.

(b) $\omega_0 = 2\pi \cdot 49.5$rad/s.

(c) $\omega_0 = 2\pi \cdot 50.5$rad/s.

(d) $\omega_0 = 2\pi \cdot 51$rad/s.

Fig. 19. Experimental results. Steady state operation under ±1Hz base frequency deviation.

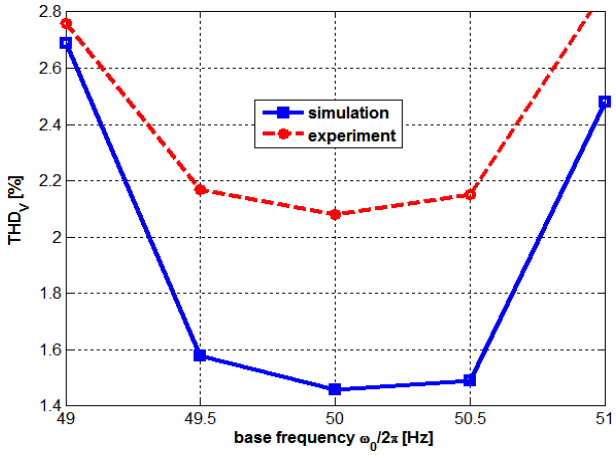


Fig. 20. Simulated and experimental THD_V under base frequency deviation.

V. CONCLUSIONS

It has been shown in the paper that it is possible to directly construct inverter output impedance utilizing uncertainty and disturbance estimator algorithm, owing to its two-degree-of-freedom structure. Once desired tracking performance is established, it is possible to shape the output impedance by selecting a proper filter. In case output impedance minimization is desired to reduce the total harmonic distortion of the output voltage, multi-band-stop filter structure may be utilized. Moreover, robustness to base frequency variation was assured by increasing the bandwidth of each filter. Nevertheless, if other output impedance manipulation is looked-for, respective filter may be in general designed. It was shown that several trade-offs exist due to limited control bandwidth and should be properly managed to achieve the best results. Theoretical findings were well-validated by experimental results.

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