Structural Resemblance Between Droop Controllers and Phase-Locked Loops

Qing-Chang Zhong, *Senior Member, IEEE*, and Dushan Boroyevich, *Fellow, IEEE*

***Abstract*—It is well known that droop control is fundamental to the operation of power systems and now the parallel operation of inverters while phase-locked loops (PLL) are widely adopted in modern electrical engineering. In this paper, it is shown at first that droop control and PLLs structurally resemble each other. This bridges the gap between the two communities working on droop control and PLLs. As a result, droop controllers and PLLs can be improved and further developed via adopting the advancements in the other field. This finding is then applied to operate the conventional droop controller for inverters with inductive output impedance to achieve the function of PLLs, without having a dedicated synchronization unit. Extensive experimental results are provided to validate the theoretical analysis.**

***Index Terms*—Droop control, enhanced phase-locked loop (PLL), sinusoidal tracking algorithm (STA), microgrid, smart grid integration, inverters, self-synchronization, parallel operation, synchronous machines, autonomous systems**

I. Introduction

In order to address the energy and sustainability issues being faced worldwide nowadays, more and more renewable energy sources are being connected to power systems, often via DC/AC converters (also called inverters) [2]. These inverters are required to synchronize with the system connected to, before and after being connected. There are many ways to synchronize an inverter with the grid but the most commonly adopted strategies are based on phase-locked loops [2]–[4], of which some examples can be found in the grid connection of renewable energy [5], [6], FACTS devices [7], [8], active power filters [9], UPS applications [10] and power quality control [11]. Phase-locked loops are also widely adopted in other areas of modern electrical engineering, e.g. communication and signal processing. A recent search from http://ieeexplore.ieee.org/ with "phase-locked loops" has found 13,000 papers.

Another important requirement for these inverters is that they should take part in the regulation of system frequency and voltage, in particular, when the penetration of renewable energy exceeds a certain level. This often requires the inverters to be operated as voltage-controlled suppliers instead of current-controlled suppliers, which currently dominate the market. What is fundamental to the operation and regulation of the frequency and voltage of a power system is the so-called droop control strategy. It was originally adopted to operate synchronous generators and have recently been adopted to operate inverters connected in parallel [12]–[21]. The generators and/or inverters change the reactive power and real power output according to the system voltage and frequency autonomously. It has also been applied in the synchronverter technology to make inverters behave like synchronous generators [22], [23]. A recent search from http://ieeexplore.ieee.org/ with "droop control" has found about 2000 papers.

To the best knowledge of the authors, no links between these two strategies have been reported in the literature. Following the conference version [1] of this paper, it is shown in this paper that these two strategies are actually closely related, which bridges the gap between the two communities. This also provides the theoretical explanation why a dedicated synchronization unit, which has been deemed to be a must-have component for grid-connected inverters, could be removed to implement self-synchronized synchronverters, as proposed in [24]. The significance of this lies in that the problem caused by (multiple) phase-locked loops [25]–[28] is removed and the system performance and reliability are improved. It also establishes a link between the two communities who are working on droop control and phase-locked loops. With comparison to the conference version [1] of this paper, a section is added to operate the conventional droop control strategy for inverters with an inductive output impedance to achieve synchronization after some minor changes, as an example to demonstrate the possible applications of the findings in this paper. Moreover, extensive experimental results are provided to validate the theoretical analysis.

In order to improve the readability, the main tool adopted in this paper is block diagrams, which are commonly used in control engineering, instead of mathematical equations. If needed, the block diagrams can be transformed into differential equations. The rest of the paper is organized as follows. The PLLs and droop control are briefly reviewed in Sections II and III, respectively, and their link is established in Section IV. The application of the findings in this paper to the conventional droop controller is shown in Section V. Experimental results are presented in Section VI, with conclusions and discussions provided in Section VII.

II. Brief Review of Phase-Locked Loops (PLL)

A basic phase-locked loop (PLL), as shown in Figure 1, adopts a control loop to track the phase of an input signal. It

A preliminary version [1] of this paper was presented at the 39th Annual Conference of the IEEE Industrial Electronics Society held in Vienna, Austria in November 2013.

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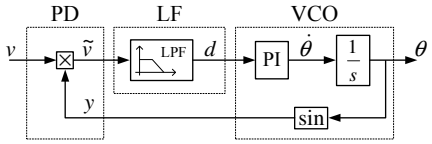


Figure 1. A basic PLL

can provide the frequency information of the signal as well, but normally without the information of the voltage amplitude.

In order also to obtain the amplitude information of the input signal, an enhanced PLL (EPLL) [29], [30] can be adopted. This method was introduced with several different names, e.g. the sinusoidal tracking algorithm (STA) [31], the amplitude phase model (APM) and amplitude phase frequency model (APFM) [32].

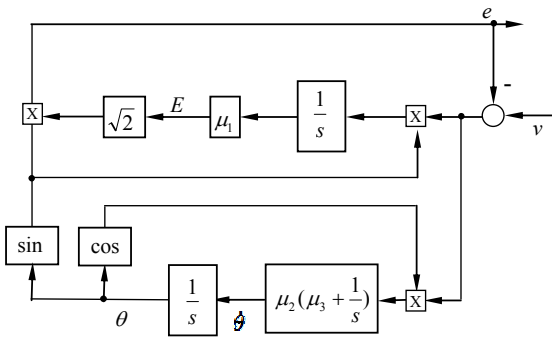


Figure 2. The enhanced phase-locked loop (EPLL) or the sinusoidal tracking algorithm (STA)

The enhanced PLL can be designed by using the gradient descent method [33]. Assume that a typical periodic voltage $v\left(t\right)$ has the general form of

$$v\left(t\right)=\sum_{i=0}^{\infty}\sqrt{2}V_{i}\sin\theta_{gi}+n\left(t\right)$$

where V_i and $\theta_{gi}=\omega_{gi}t+\delta$ are the RMS value and phase of the i-th harmonic component of the voltage, and $n(t)$ represents the noise on the signal. The objective of a PLL can be regarded as extracting the component $e\left(t\right)$ of interest, which is usually the fundamental component, from the input signal $v\left(t\right)$. Denote the estimated or recovered signal $e(t)$ as

$$e\left(t\right)=\sqrt{2}E\left(t\right)\sin(\int_{0}^{t}\omega\left(\tau\right)\mathrm{d}\tau+\delta\left(t\right)),$$

where $E\left(t\right)$ is the estimated RMS voltage, $\omega\left(t\right)$ is the estimated frequency and $\theta\left(t\right)=\int_{0}^{t}\omega\left(\tau\right)\mathrm{d}\tau+\delta\left(t\right)$ is the estimated phase of $e\left(t\right)$. Then the problem of designing a PLL can be formulated as finding the optimal vector $\psi(t)=\left[\begin{array}{ccc}E(t) & \omega(t) & \delta(t)\end{array}\right]^{T}$ that minimizes the cost function

$$J\left(\psi\left(t\right),t\right)=\frac{1}{2}d^{2}\left(t\right)=\frac{1}{2}\left[v\left(t\right)-e\left(t\right)\right]^{2},$$

where $d\left(t\right)=v(t)-e(t)$ is the tracking error. According to the gradient descent method [33], this optimization problem can be solved via formulating

$$\frac{\mathrm{d}\psi\left(t\right)}{\mathrm{d}t}=-\mu\frac{\partial J\left(\psi\left(t\right),t\right)}{\partial\psi\left(t\right)}$$

where μ is the diagonal matrix $diag\{\frac{1}{2}\mu_1,\ \frac{1}{2}\mu_2,\ \mu_3\}$ chosen to minimize J along the direction of $-\frac{\partial J(\psi(t),t)}{\partial\psi(t)}$. The resulting set of differential equations can be found as [31], [32]

$$\left\{\begin{array}{l}\frac{\mathrm{d}E(t)}{\mathrm{d}t}=\mu_{1}d\sin\theta,\\ \frac{\mathrm{d}\omega(t)}{\mathrm{d}t}=\mu_{2}Ed\cos\theta,\\ \frac{\mathrm{d}\theta(t)}{\mathrm{d}t}=\omega+\mu_{3}\frac{\mathrm{d}\omega}{\mathrm{d}t}.\end{array}\right.\tag{1}$$

Since the variation of E is relatively small with comparison to the variation of d, the major dynamics of $\omega(t)$ is from d and the effect of E can then be combined with the proper selection of μ_2. As a result, the enhanced PLL can be constructed as shown in Figure 2.

Comparing the enhanced PLL shown in Figure 2 to the basic PLL shown in Figure 1, it can be seen that the enhanced PLL contains an amplitude channel to estimate the amplitude of the input signal, in addition to the frequency channel that is very similar to the basic PLL.

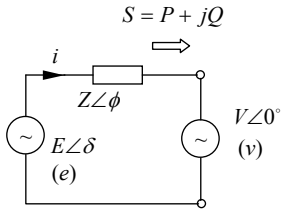
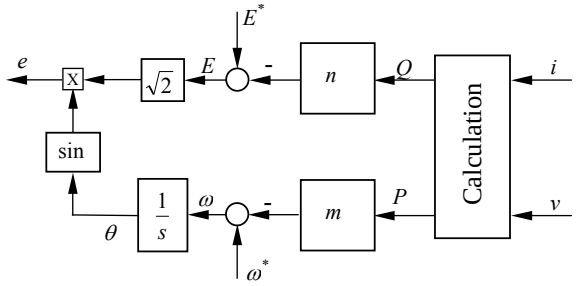
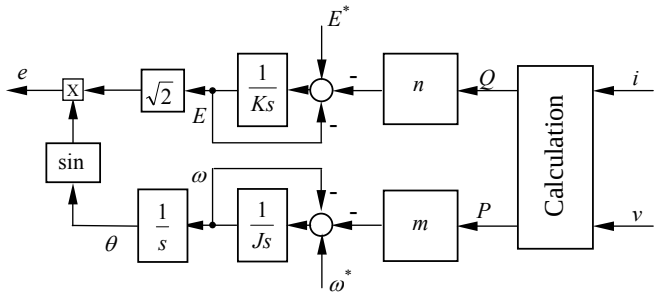


Figure 3. Power delivered to a voltage source through an impedance



(a) without considering the integral effect



(b) with the hidden integral effect explicitly considered

Figure 4. Conventional droop control scheme (for inductive impedance)

III. Brief Review of Droop Control

Figure 3 illustrates a voltage source $e=\sqrt{2}E\sin\theta$ with $\theta=\omega t+\delta$ delivering power to another voltage source (terminal) $v=\sqrt{2}V\sin\omega t$ through an impedance $Z\angle\phi$. The voltage

source could be a conventional synchronous generator or a voltage-controlled inverter. Since the current flowing through the impedance is

$$\begin{aligned}\bar{I} &= \frac{E\angle\delta - V\angle 0^\circ}{Z\angle\phi} \\ &= \frac{E\cos\delta - V + jE\sin\delta}{Z\angle\phi},\end{aligned}$$

the real power and reactive power delivered by the source to the terminal via the impedance can be obtained as

$$\begin{aligned}P &= (\frac{EV}{Z}\cos\delta - \frac{V^2}{Z})\cos\phi + \frac{EV}{Z}\sin\delta\sin\phi, \\ Q &= (\frac{EV}{Z}\cos\delta - \frac{V^2}{Z})\sin\phi - \frac{EV}{Z}\sin\delta\cos\phi,\end{aligned}$$

where δ is the phase difference between the supply and the terminal, often called the power angle. This is the basis of the droop control [2], [15], [34]–[37], that is widely adopted in power systems and recently in parallel-operated inverters.

When the impedance is inductive, $\phi = 90^\circ$. Then

$$P = \frac{EV}{Z}\sin\delta \quad \text{and} \quad Q = \frac{EV}{Z}\cos\delta - \frac{V^2}{Z}.$$

When δ is small, there are

$$P \approx \frac{EV}{Z}\delta \quad \text{and} \quad Q \approx \frac{V}{Z}E - \frac{V^2}{Z},$$

and, roughly,

$$P \sim \delta \quad \text{and} \quad Q \sim E.$$

As a result, the conventional droop control strategy for an inductive Z takes the form

$$E = E^* - nQ, \tag{2}$$

$$\omega = \omega^* - mP, \tag{3}$$

where E^* is the rated RMS system voltage. This strategy, as shown in Figure 4(a), consists of the $Q-E$ and $P-\omega$ droop, i.e., the voltage E is regulated by controlling the reactive power Q and the frequency f is regulated by controlling the real power P.

The droop control strategy takes different forms when the impedance is of different types [2], [21]. When the impedance is capacitive, the droop control still takes the form of $Q-E$ and $P-\omega$ droop but with positive signs. When the impedance is resistive, the droop control takes the form of $Q-\omega$ and $P-E$ droop. Note that the (output) impedance of an inverter is normally inductive but can be changed to resistive or capacitive; see [2], [38] for more details. The conventional droop control strategy has some fundamental limitations and is not able to maintain accurate sharing of both real power and reactive power when there are component mismatches, parameter shifts, numerical error, disturbances and noise etc. A robust droop controller is presented in [2], [12] to overcome these issues, which has recently been shown to be universal for inverters with different types of output impedance [21]. These do not affect what is discussed in this paper so the analysis will be based on the conventional droop control strategy for the sake of simplicity.

IV. The Structural Resemblance between Droop Control and Phase-Locked Loops

A. When the Impedance is Inductive

One insightful observation about droop control pointed out in [12] is that the voltage droop control actually includes an integrator because E can be obtained via dynamically integrating

$$\Delta E \triangleq E^* - E - nQ$$

until $\Delta E = 0$ instead of setting $E = E^* - nQ$ statically. This is also true for the frequency droop control, where the frequency ω can be obtained via integrating

$$\Delta\omega \triangleq \omega^* - \omega - mP$$

until $\Delta\omega = 0$. The droop control strategy with this hidden integral effect explicitly considered is shown in Figure 4(b), where the integral time constants are chosen as J and K for the frequency and voltage channels, respectively. This is equivalent to adding a low-pass filter $\frac{1}{Js+1}$ to the frequency (real power) channel and a low-pass filter $\frac{1}{Ks+1}$ to the voltage (reactive power) channel shown in Figure 4(a), respectively. In the steady state, the inputs to the integrators are zero, which recovers the droop control strategy (2-3). Apparently, Figure 4(b) becomes Figure 4(a) when the integral time constants are chosen as $K = 0$ and $J = 0$.

The current i flowing through the impedance $Z = Ls + R$ in Figure 3 is

$$i = -\frac{v - e}{Ls + R}.$$

This can be adopted to close the loop between v and e in Figure 4(b), as shown in Figure 5. Note that $i = 0$ when $e = v$ and, in this case, the voltage e accurately recovers or estimates the voltage v. In other words, the voltage e is synchronized with the input v.

Normally, the real power P and reactive power Q are calculated via measuring the terminal voltage v and the current i. Actually, it is better to use the voltage e than the terminal voltage v for this purpose because e is available internally. This leaves out the power losses of the filter inductor but it does not matter. The physical meaning of this is to droop the voltage and frequency according to the real power and the reactive power generated by the voltage source e. To some extent, this is more reasonable than using the terminal voltage v because it reflects the genuine real power and reactive power delivered by the voltage source e. In this case, the real power is

$$P = \frac{1}{T}\int_{t-T}^{t} e \times i \,\mathrm{d}t, \tag{4}$$

where T is the period of the system. Applying the Laplace transform, this is equivalent to passing the instantaneous real power $p = e \times i$ through the hold filter

$$H(s) = \frac{1 - e^{-Ts}}{Ts}$$

to obtain the (averaged) real power P. The reactive power can be obtained similarly. Define the voltage

$$e_q = \sqrt{2}E\sin(\theta - \frac{\pi}{2}) = -\sqrt{2}E\cos\theta,$$

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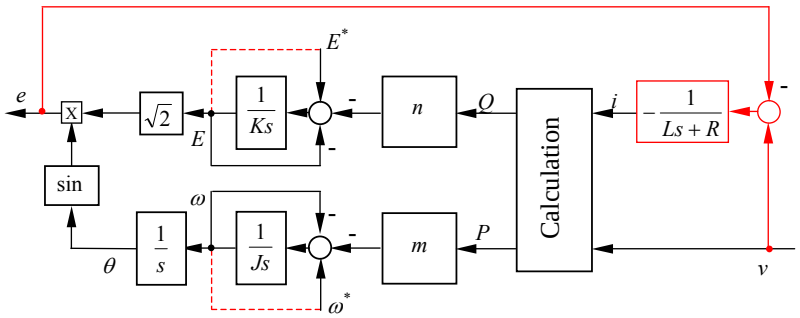


Figure 5. The droop controller shown in Figure 4(b) with the (inductive) impedance taken into account

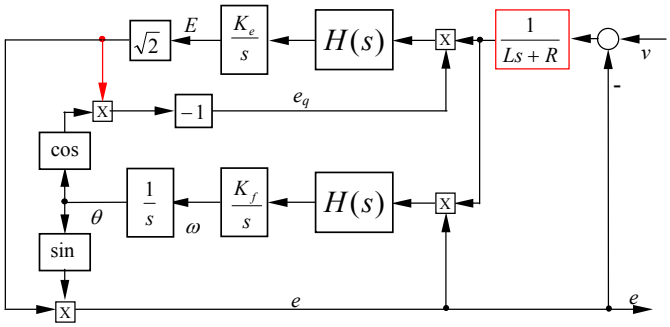
which has the same amplitude as e but with a phase angle delayed by $\frac{\pi}{2}$ rad. Then, the reactive power can be calculated as

$$Q = \frac{1}{T}\int_{t-T}^{t} e_q \times i \, \mathrm{d}t. \tag{5}$$

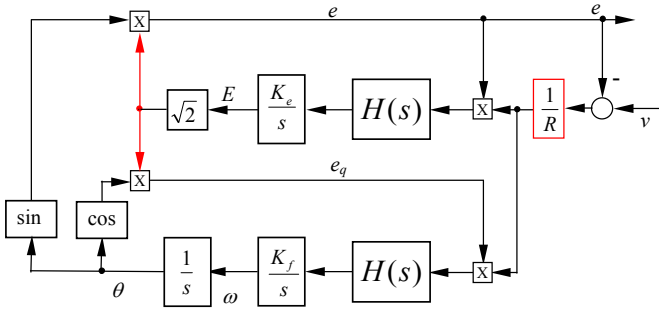
For example, for the current $i = \sqrt{2}I\sin\theta_i$, there is

$$Q = \frac{1}{T}\int_{t-T}^{t} 2EI\sin(\theta - \frac{\pi}{2})\sin\theta_i \mathrm{d}t = EI\sin(\theta - \theta_i),$$

which is indeed the reactive power generated by $e = \sqrt{2}E\sin(\theta)$ and i. Note that it is not compulsory to use the hold filter. A low-pass filter with the appropriate bandwidth could be used as well. This does not affect the main reasoning here.



(a) when the impedance is inductive



(b) when the impedance is resistive

Figure 6. Droop control strategies in the form of a phase-locked loop

When the droop controller is operated in the droop mode, the voltage set-point E^* and the frequency set-point ω^* can be set as the rated system values whether it is connected to the grid or it is operated in the standalone mode. They can also be set as the grid voltage E and the grid frequency ω for grid-connected applications to send the desired real power P_{set} and reactive power Q_{set} to the grid (this is not shown in Figure 5 but can be easily implemented by changing $-P$ to $P_{set} - P$ and $-Q$ to $Q_{set} - Q$). If E^* is set as E and ω^* is set as ω[1], as shown in Figure 5 by the dashed lines, then the voltage e is the same as v in the steady state. This effectively cancels the loop around the integrators $\frac{1}{Js}$ and $\frac{1}{Ks}$. Hence, the block diagram shown in Figure 5 can be redrawn as shown in Figure 6(a), after connecting the dashed lines and calculating the power by using e, as described in (4) and (5). The gains are lumped as $K_e = \frac{n}{K}$ and $K_f = \frac{m}{J}$. This is similar to the widely-used enhanced PLL [29], [30] or the sinusoid-tracking algorithm [31], [39] (which are essentially the same) shown in Figure 2, apart from three major differences: 1) the sin and cos functions are swapped; 2) there is a low-pass filter $\frac{1}{Ls+R}$, or an integrator when $R = 0$; 3) there is a negative sign in the amplitude channel of Figure 6(a). The hold filter $H(s)$ is to filter out the ripples and could/should be inserted into the EPLL/STA to improve the performance so it does not cause any major difference. Note that, when there is no power exchanged with the grid, a droop controller actually behaves like an PLL and achieves synchronization with $e = v$. When the amplitude channel is not considered, the frequency channel is the same as the basic PLL shown in Figure 1. In other words, the frequency droop control structurally resembles the basic PLL.

B. When the Impedance is Resistive

When the impedance Z is resistive, $\phi = 0°$. Then

$$P = \frac{EV}{Z}\cos\delta - \frac{V^2}{Z} \quad \text{and} \quad Q = -\frac{EV}{Z}\sin\delta.$$

When δ is small, there are

$$P \approx \frac{EV}{Z}\delta - \frac{V^2}{Z} \quad \text{and} \quad Q \approx -\frac{EV}{Z}\delta,$$

and, roughly,

$$P \sim E \quad \text{and} \quad Q \sim -\delta.$$

[1]Note that this just changes the operational point of the controller, without changing its structure.

As a result, the conventional droop control strategy for resistive impedance takes the form

$$E = E^* - nP,$$
$$\omega = \omega^* + mQ.$$

The difference from the inductive case is that the positions of P and Q are swapped and the sign before Q is changed to positive.

Following the same reasoning in the previous section, this droop controller can be described in the form of a phase-locked loop as shown in Figure 6(b). Comparing it to the enhanced PLL or the STA shown in Figure 2, they are structurally the same, without any major difference. As explained before, the hold filter $H(s)$ is to filter out the ripples and could/should be included in the STA or EPLL to improve the performance so it does not cause any major difference. If the parameters are selected as $R = E$, $\mu_1 = K_e$, $\mu_2 = K_f$ and $\mu_3 = 0$, and the hold filter $H(s)$ is removed, then the two diagrams are exactly the same. In other words, this droop controller structurally resembles an enhanced phase-locked loop. It behaves as an enhanced phase-locked loop when there is no power exchanged with the terminal and it functions as a droop controller when it exchanges power with the terminal. As a result, the same droop controller can be utilized as a synchronization unit to achieve per-synchronization and then as a droop controller to regulate the power flow. Again, when the amplitude channel is not considered, the frequency channel is more or less the same as the basic PLL shown in Figure 1. In other words, the frequency droop control structurally resembles the basic PLL.

V. Operation of the Droop Controller to Achieve Synchronization

In order to demonstrate the findings in this paper, the droop controller shown in Figure 4(a) for inverters with inductive output impedance is slightly changed so that the synchronization function can be explicitly demonstrated. As shown in Figure 7, two integrators are added to the voltage channel and the frequency channel, one each, to make the hidden integral effect explicit. A virtual impedance $sL + R$ is added to generate the virtual current i_v according to the voltage difference $v_o - v_g$. The current feeding into the power calculation block can be the grid current i_g or the virtual current i_v. The two integrators can be enabled or disabled by switches S_P and S_Q, respectively. This allows the droop controller to work in the synchronization mode or the set mode (sending P_{set} and Q_{set} to the grid), in addition to the normal droop mode (changing the real power and reactive power according to the grid frequency and voltage). In the synchronization mode, the virtual current i_v is used because the inverter is not connected to the grid and the grid current i_g is 0. After the inverter is synchronized with the grid, the circuit breaker can be turned ON. When the circuit breaker is ON, the switch S_c should be turned to Position g so that the grid current i_g is fed into the power calculation block, which operates the inverter in the set mode. Then, if needed, the switches S_P and S_Q can be turned ON to operate the inverter in the droop mode. The operation modes are summarized as shown in Table I. Note that the switches S_P and S_Q can be operated independently when the switch S_c is at Position g so it is possible to operate the real power and the reactive power in the set mode or the droop mode independently.

Table I
Operation Modes

Mode	Switch S_C	Switch S_P	Switch S_Q
Synchronization mode	s	OFF	OFF
Set mode	g	OFF	OFF
Droop mode	g	ON	ON

VI. Experimental Validation

A single-phase inverter controlled by the controller shown in Figure 7 was built and tested. The parameters of the system are shown in Table II. The control circuit of the system was constructed based on TMS320F28335 DSP, with the sampling frequency of 4 kHz. The droop coefficients used in the experiments are calculated as $n = \frac{0.1K_eE^*}{S}$ and $m = \frac{0.01\omega^*}{S}$, where S is the rated apparent power of the inverter, according to [12], so that 10% increase of the voltage E results in 100% decrease of the reactive power Q and 1% increase of the frequency f results in 100% decrease of the real power P.

Table II
Parameters of the Inverter

Parameters	Values
Grid voltage (RMS)	110 V
Line frequency f	50 Hz
Switching frequency f_s	19 kHz
DC-bus voltage V_{DC}	200 V
Rated apparent power S	300 VA
Inductance L_s	2.2 mH
Resistance R_s	0.2 Ω
Inductance L_g	2.2 mH
Resistance R_g	0.2 Ω
Capacitance C	10 μF

A. Synchronization with the Grid

The time needed for synchronization is different for different voltage v_g. Here, two typical cases with $v_g = 0$ and $v_g = V_g$ are considered. The corresponding results are shown in Figure 8(a) and (b), respectively. For the case with $v_g = 0$ when the synchronization was started, as shown in Figure 8(a), the voltage difference between the output voltage and the grid voltage, i.e., $v_o - v_g$, quickly became very small. It took less than one cycle for the whole synchronization process. For the case with $v_g = V_g$ when the synchronization was started, as shown in Figure 8(b), the synchronization took longer, about 12 cycles. This is still acceptable for grid-connected inverters. This shows indeed the droop controller can be applied to achieve synchronization before connecting the inverter to the grid, without the need of a dedicated synchronization unit.

B. Connection to the Grid

After the synchronization process is finished, the inverter is ready to be connected to the grid. This involves turning the

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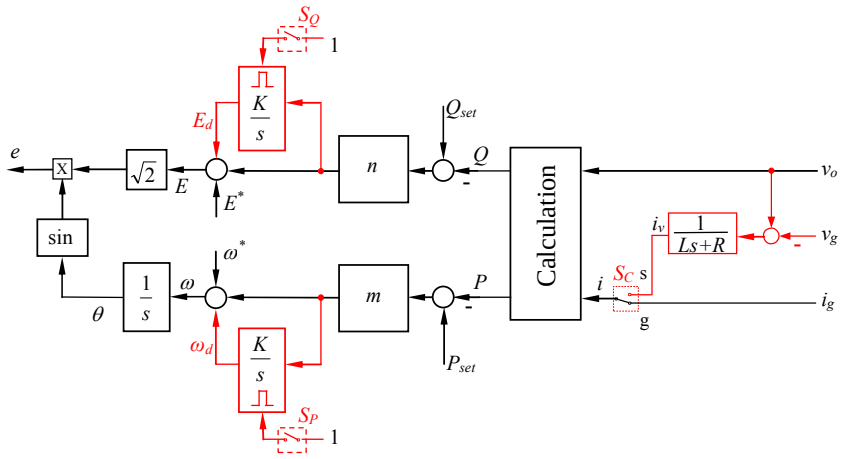
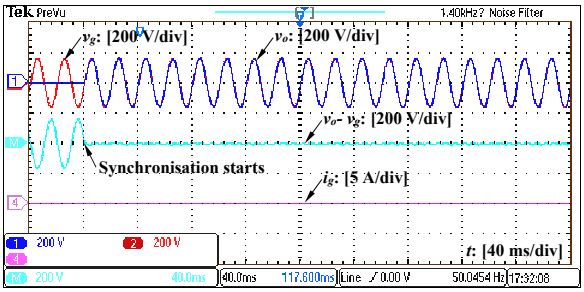
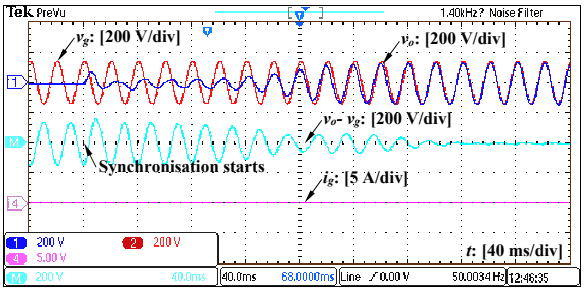


Figure 7. The conventional droop controller shown in Figure 4(a) after adding two integrators and a virtual impedance.



(a)



(b)

Figure 8. The synchronization of the droop controller shown in Figure 7: (a) when v_g crosses 0; (b) when v_g is at the peak value V_g.

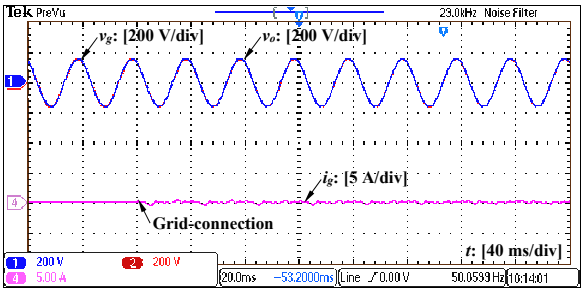


Figure 9. Connection of the droop controlled inverter to the grid

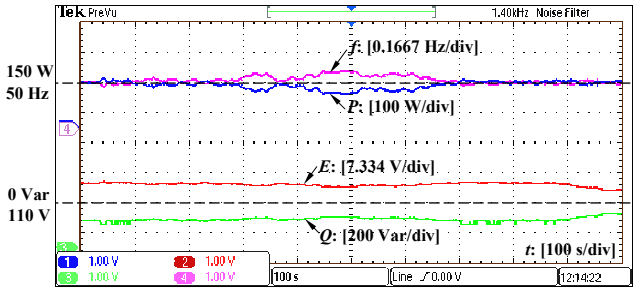


Figure 10. Regulation of the grid frequency and voltage in the droop mode.

relay ON and the switch S_C to the Position g, which shifts the current used for calculating P and Q from the virtual current i_v to the grid current i_g. As shown in Figure 9, the grid current i_g was well maintained around zero without large spikes, as expected because $P_{set} = 0$ and $Q_{set} = 0$.

C. Operation in the Droop Mode

In order to test the droop function of regulating P and Q corresponding to the variations of f and E, the inverter was continuously operated in the droop mode while being connected to the public grid. The results are shown in Figure 10. The real power P is almost symmetrical to the grid frequency f while the reactive power Q is symmetrical to the voltage E, as expected. When the frequency is higher (lower) than the rated frequency, the real power is automatically reduced (increased) proportionally. Similar regulation capability can be seen from the reactive power against the voltage. It is worthy emphasizing that the inverter kept in synchronization with the grid after being connected to the grid, without a dedicated synchronization unit. The synchronization is achieved by the droop controller itself. The voltage did not change much during the experiment but the trend is very clear.

D. Robustness of Synchronization

In order to test the robustness of the synchronization, the DC-bus voltage V_{DC} was changed when the system was operated in the set mode with $P_{set} = 150\,\text{W}$ and $Q_{set} = 150\,\text{Var}$. At first, V_{DC} was suddenly dropped from $200\,\text{V}$ to $180\,\text{V}$. As shown in Figure 11(a), there was no problem with the synchronization. The grid current i_g dropped initially because

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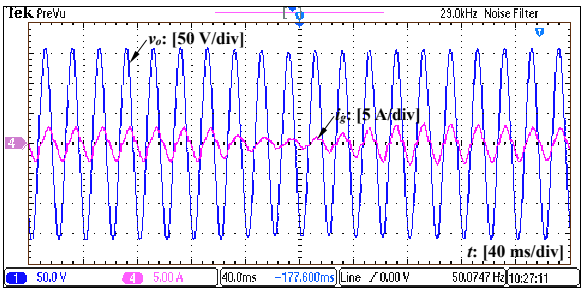
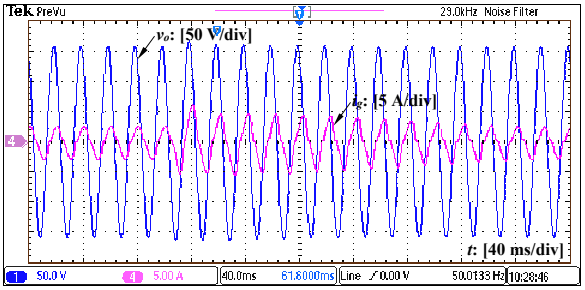


(a)



(b)

Figure 11. Robustness of synchronization against DC-bus voltage changes: (a) when the DC-bus voltage V_{DC} was changed from 200 V to 180 V and (b) when the DC-bus voltage V_{DC} was changed from 180 V to 200 V.

of the dropped V_{DC} but, after about 10 cycles, it recovered to the original value before the voltage change to maintain the real power and reactive power sent to the grid. Then, V_{DC} was suddenly increased from 180 V to 200 V. Again, there was no problem with the synchronization, as shown in Figure 11(b). The grid current i_g increased initially but after about 10 cycles it recovered to the original value before the voltage change.

E. When the Operation Mode was Changed

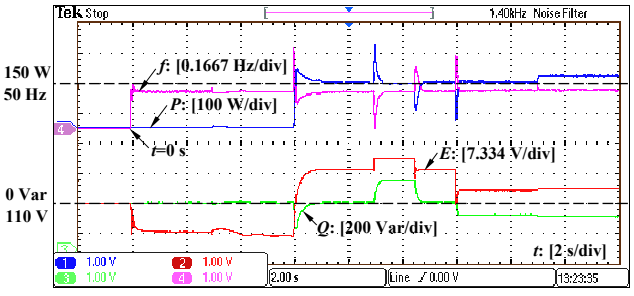


Figure 12. System responses when the operation mode was changed

The frequency, voltage, real power and reactive power of the system when the mode of the droop controller was changed in the sequence of the synchronization mode, connection to the grid, the set mode and the droop mode are shown in Figure 12. At $t = 0$ s, the synchronization was enabled. As shown in Figure 12, both the real power and the reactive power were controlled around zero. When the inverter was connected to the grid at 3 s, there was not much transient and both the real and reactive power were maintained around zero. The real and reactive power references were changed at $t = 6$ s and $t = 9$ s to 150 W and 150 Var, respectively. The real power and reactive power responded quickly, with some coupling effect. There was some dynamics in the frequency but it settled down. The voltage E increased because of the increased real power and then the increased reactive power output. At $t = 10.5$ s, Q_{set} was changed back to 0. At $t = 12$ s, the droop mode was enabled for the reactive power. The reactive power started changing according to the voltage, nearly symmetrically. At $t = 15$ s, the droop mode was enabled for the real power. The real power started changing according to the frequency, nearly symmetrically as well. This has demonstrated that the droop controller with the changes shown in Figure 7 can function properly without a dedicated synchronization unit.

VII. Conclusions

In this paper, it has been shown that a droop controller structurally resembles an enhanced phase-locked loop. This builds up a link between the droop control community and the PLL community, and offers fundamental understanding about the operation of power systems dominated by droop-controlled renewable energy sources interfaced by inverters. As a result, there is no need to have a extra synchronization unit in addition to the droop controller for synchronization. The link is shown for the case when the impedance is resistive, but can be easily extended to investigate the cases when the impedance is inductive or capacitive to find the equivalent structure of phase-locked loops. Indeed, the case with inductive output impedance has been demonstrated by extensive experimental results.

What is described in this paper actually provides the theoretical explanation why a dedicated synchronization unit for grid-connected inverters that has been deemed to be a must-have component for grid-connected inverters [40] can be completely removed, as demonstrated in [24] for the first time. Because of the inherent synchronization mechanism of droop control strategies revealed in this paper, there is no longer a need to use a phase-locked loop in conjunction with a droop controller and a droop controller can be used for synchronization as well. In other words, the synchronization function and the power sharing function of an inverter can be integrated in a droop controller. This avoids the problems brought by PLL to grid-tied inverters, e.g. competing with each other, difficulties in tuning PLLs and performance degradation etc.

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