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Time-Division Multiplexing for Cable Reduction
In Ultrasound Imaging Catheters

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Abstract — In ultrasound imaging catheter applications, gathering the data from multi-element transducer arrays is difficult as there is a restriction on cable count due to the diameter of the catheter. In such applications, CMUT-on-CMOS technology allows for 2D arrays with many elements to be designed and bonded directly onto CMOS circuitry. This allows for complex electronics to be placed at the tip of the catheter which leads to the possibility to include electronic multiplexing techniques to greatly reduce the cable count required for a large element array. Current approaches to cable reduction tend to rely on area and power hungry circuits to function, making them unsuitable for use in catheters. Furthermore the length requirement for catheters and lack of power available to on-chip cable drivers leads to limited signal strength at the receiver end. In this paper an alternative approach using Analogue Time Division Multiplexing (TDM) is presented, which addresses the cable restrictions of the catheter and, using a novel digital demultiplexing technique, allows for a reduction in the number of analogue signal processing stages required.

Keywords — CMUT Electronics; TDM; CMUT-on-CMOS; ICE

I. INTRODUCTION

Intracardiac Echocardiography (ICE) catheters provide a unique method to image the functional operation of the heart. Catheter based real-time 3D imaging requires data to be captured from many transducer elements simultaneously to avoid motion artefacts. Unlike conventional ultrasound methods, ICE is limited in terms of cable count due to size constraints of the catheter. Current ICE devices have limited 3D view and require harmful X-ray imaging for navigation. Using a CMUT-on-CMOS approach [1], an alternative catheter which is MRI compatible would eliminate exposing the patient to harmful radiation. To achieve such a catheter, a method for connecting a CMUT array with many elements to the imaging system using a limited cable count is needed. Using a CMUT-on-CMOS approach, complex electronics for channel multiplexing and transmit beamforming can be integrated with a standard CMUT transducer. This on-chip multiplexing allows for a significant reduction of number of electrical connections.

II. CHANNEL MULTIPLEXING METHODS

Many different approaches to reducing cable count were considered. One of the options is on-chip digital modulation, however this would require a large number of A/D converters on the tip of the catheter which is not feasible due to size constraints and electrical power requirements.

Another approach, which involves performing partial beamforming (μ-Beamforming) using on-chip analogue delays, has been used with ultrasound transducers to reduce the number of receiver cables as demonstrated in [2] and [3]. However, this approach requires a large number of capacitors and switches for each channel in order to achieve the required analogue delays, and thus the space requirements eliminate this as an option for the ICE devices.

A third approach for cable reduction is Frequency Division Multiplexing. This method has been shown to be feasible for ICE applications [4] but requires a band-pass filter to be implemented for each CMUT element to prevent interference. These filters are sensitive to silicon process variations and so require tuning after manufacture. This would require multiple on chip tuning circuits and require each transducer to be calibrated prior to being assembled onto a catheter. Furthermore, FDM would require additional complex hardware and software (Analogue or DSP) to demodulate and recover the signals prior to image reconstruction.

Time-Division Multiplexing (TDM) is the cable reduction scheme that was selected for this application. In TDM, the channels are multiplexed in time, with each channel being assigned a time slot in which to transmit. This method was demonstrated in [5] to be a viable option for multiplexing channels in CMUT applications. In that paper, the scheme is demonstrated in static-multiplexing whereby multiple transmit firings are required to image with the entire array, with the selected channel for each cable being changed on each firing [1, 5]. However this could cause motion artefacts in the image. A TDM approach is also present in [5] for a dynamic-multiplexing scheme where data from all elements is collected in a single firing by rapidly counting through channels, such that all are individually sampled at above the Nyquist rate.

III. PROPOSED TDM APPROACH

In this application, the dynamic-multiplexing approach is required. In order to 3D image while limiting motion artefacts, reflection data for all channels must be captured in a single transmit firing. This requires enough bandwidth in the electronics and cabling to carry the multiplexed signal – of at least the bandwidth per channel multiplied by the number of channels per cable. As an example, multiplexing eight 7MHz 80% bandwidth CMUT devices would require at least 10MHz per channel, or over 80MHz minimum channel bandwidth.
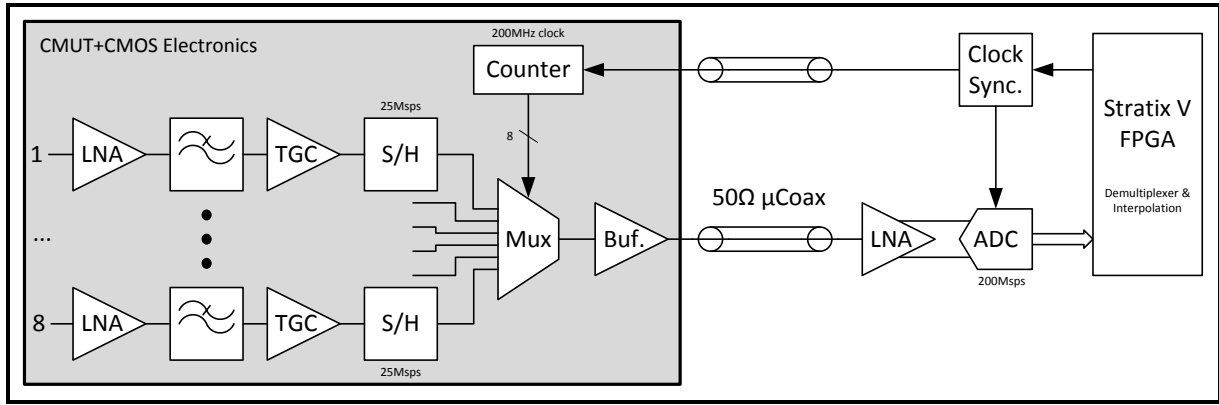
Fig. 1. Analogue Time-Division Multiplexing Scheme using Digital Demultiplexing. Frequencies shown are used in the tested 8-channel system. The shaded region indicates the CMUT-on-CMOS electronics on the chip at the catheter tip.

A minimal TDM transmit system requires only an analogue multiplexer and a buffer for each channel and so requires much less space to implement than the other channel reduction schemes considered. However at the receiver end of the cable the signals need to be demultiplexed. If done in the analogue domain this would require buffering, switching, filtering, and ADCs for each channel. Each of these stages would add additional noise to the system, especially problematic due to the restrictions of power available to the buffers driving the long narrow cables in the catheter. There would also be added complexity in matching these circuits across all channels.

A novel approach to Analogue TDM has been developed (Fig. 1) which eliminates the need for demultiplexing to be performed in the analogue domain, resulting in both a reduction of the number of ADCs required and also removal of the analogue switch and filters required in the standard design.

By using a high speed ADC which is capable of sampling at the same frequency as the TDM clock signal, the system can be designed such that each ADC sample corresponds exactly to one channel in the multiplexed data. This means that as the samples are taken, demultiplexing becomes a simple task of separating the data into groups consisting of every n^{th} sample. This results in a data stream for each TDM channel which can then be filtered and interpolated using DSP techniques.

To reduce issues of settling time of the buffers and ADC, the sample and hold (S/H) circuitry, normally located in the ADC, has been relocated to the catheter electronics, being performed on chip before the TDM multiplexer. Each channel has its own S/H buffer which runs at $1/n$ times the speed of the ADC sample rate which means there is a longer period of time for the signal to settle in the hold capacitor, and a stable signal is transmitted down the cable in each sample period.

The multiplexing process is such that there is a counter on-chip which is driven by the sample clock. This counter selects each channel in turn, allowing for a short dead period between channels to prevent the shorting of channels during switchover. When a channel is selected, the hold capacitor in its S/H buffer is disconnected from the CMUT analogue front end (AFE) and connected through the analogue multiplexer to a buffer which drives a micro-coaxial cable running the length of the catheter to the ADC.
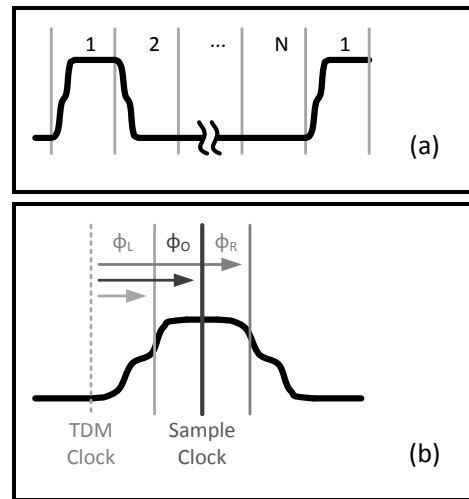

Fig. 2 (a) Training Sequence to identify channel 1

(b) Locating optimal phase between TDM and sample clocks to ensure not sampling during channel switching transient.

Alignment is required between the TDM multiplexer and the ADC to ensure that the data can be correctly demultiplexed and the quantised value is a true representation and not a conversion of the transition between channels. This is achieved using a two stage training sequence. During the sequence, the first channel is fixed to one bias rail and the others fixed to a different bias rail just before the multiplexer. By analysing the converted data it is possible to identify the first channel by way of the quantised codes being significantly different in one sample than the others as illustrated in Fig. 2(a).

Once the first channel is identified, the TDM clock phase can be adjusted using a PLL in the FPGA to determine the optimum alignment, as shown in Fig. 2(b). By locating the phases where the value of the first channel begins to fall away, ϕ_L and ϕ_R, the transition points are identified. The optimal phase where the sampling should be performed, ϕ_O, can then be found as the midpoint. The phase shift added will then account for any propagation delays in the system, including the delay in the cables carrying the clock to the CMOS IC and those carrying the multiplexed signals back.
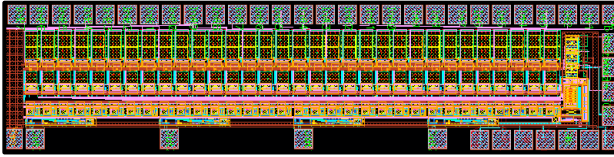
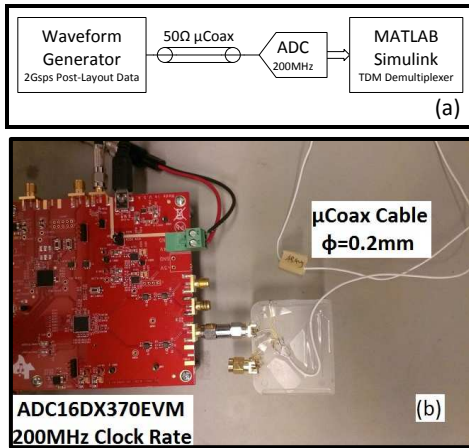Fig. 3   CMOS Implementation of TDM and Analogue Front End

Fig. 4   (a) Diagram of Experimental Setup

(b) Photograph of Coax and ADC setup

IV.   TDM Implementation in CMOS

The proposed multiplexing scheme and analogue front end has been implemented for a 32 channel CMUT device, utilising four 8:1 TDM multiplexers and so requiring only 4 cables. The circuit is designed to be interfaced with CMUT devices with a 7MHz centre frequency with 80% fractional bandwidth and as such a sampling rate for each channel of 25Msps was selected to ensure sampling above the Nyquist rate.

The TDM design from Fig. 1 has been designed for a 0.18μm 60V 1P4M TowerJazz CMOS process will operate from a 1.8V supply. The implemented circuitry, shown in Fig. 3, occupies an area of 3.25mm by 0.55mm and as such would require only a small portion of the space available at the tip of a catheter. Based on post layout simulations, the circuit has an estimated peak operating power of 140mW. The first stage of the AFE is an LNA with 16dB of gain over a bandwidth of 12MHz and a noise voltage of 25μV integrated over that range. The designed bandwidth of the LNA coupled with the frequency response of the CMUT devices act in essence as a low pass filter, limiting the signal bandwidth to avoid aliasing when the signal is sampled. The next stage of the chain is a 4 level TGC circuit to improve the dynamic range of the system by up to 12dB. This is then fed into a sample-and-hold buffer to sample the signals at 25MHz ready to be multiplexed. Each buffer also has a controllable pull up or down resistor which can be enabled to generate the link training sequence. A digital counter is implemented which controls when the hold capacitor for each channel is selected by an analogue multiplexer. The final output stage is a current feedback buffer adopted from [6] which has an output bandwidth of 800MHz when driving a 50Ω‖15pF load.

V.   Experimental Setup and Results

To demonstrate the proposed TDM approach prior to silicon manufacture, the behaviour of the CMOS design was simulated using Cadence. To determine the usability of the TDM scheme, the effect of the coax cable, ADC and digital demultiplexing must also be considered. To facilitate this, an Agilent Technologies 81150A Arbitrary Waveform Generator (AWG) has been used as a stand-in for the analogue front end silicon to drive a 1 metre sample of 48awg μCoax cable suitable for use in a catheter. The data is then sampled by a Texas Instruments ADC16DX370 device clocked at 200MHz. Finally the captured data is run through a MATLAB Simulink model which separates the samples into 8 data streams and then passes each through a Bandpass filter and interpolation filter. Fig. 4(a) and (b) show a diagram and photograph of the setup. It is important to note that the FIR filters designed and used in the Simulink model are fully representative of what can and would be implemented in an FPGA. In this setup, link training was performed manually by observing the sampled data and adjusting the phase of the AWG to correct alignment, but the process used was the same as described in Fig. 2.

For this experiment the stimulus used for the post layout simulation, i.e. the signals for each channel fed into the LNA inputs, is shown in Fig. 5(a). These waveforms are 7MHz centre frequency Gaussian pulses with an 80% bandwidth with various amplitudes and phases. These waveforms represent a worst case scenario in which the signals from each channel are out of phase in a way which results in large differences between channels in the multiplexed output. In this scenario crosstalk will be maximised due to longer transition times between channels due to the larger voltage swings. The resulting simulation output data stream is shown in Fig. 5(b).

Fig. 5(c) shows the demultiplexed data that was extracted from the Simulink model. From initial inspection it can be seen that the system is correctly demultiplexing the channels and recovering 8 signals. On closer inspection it can be seen that the recovered signals are however not identical to the original. This is made apparent in Fig. 5(d) in which a comparison is made between the input and output signals for channel 4 and also for channel 8. Analysing these signals, it can be determined that there is approximately 23dB difference between the signal amplitude and that of the distortion.

The discrepancy in the signal appears to be as a result of crosstalk caused by transmission line reflections in the coaxial cable. It was concluded from observations that the distortion is affecting the amplitude of the signals in an asymmetric manner and crucially that the additional peaks distorting each channel are not directly aligned the peaks in adjacent channels as would be expected if the issue was due simply to adjacent channels bleeding together due to lack of cable bandwidth.

Upon further testing with the cable, by connecting one end to a 50Ohm terminated oscilloscope input and sending the training sequence from the AWG, clear reflections can be observed. Much of this reflection can be compensated for by ensuring that when the cable is connected to the ADC circuitry it is done so using microstrip traces with carefully matched impedance.

VI. CONCLUSION

In this paper, a novel approach has been presented in which Analogue Time Division Multiplexing can be employed for use in transferring signals from a CMUT array with a large number of elements through an ICE catheter with a limited cable count. Existing methods of channel reduction were considered in section II, but were determined to be unsuitable for use in a CMUT based ICE system for reasons varying from space requirements to complexity. TDM was determined to be the most suitable approach for this design, though limitations of power requirements and cable length implications of catheter applications required an alternative approach to the structure of the multiplexing scheme to fully meet the needs of this application.

The proposed design for a multiplexing circuit coupled directly with multiple AFEs in a way which would be suitable for use in a CMUT-on-CMOS process been implemented in a $0.18\mu m$ 60V CMOS process. Each transducer element could be placed above its corresponding AFE to maximise integration and reduce space requirements in a future design. Based on post-layout simulation of this design experimentation has been carried to determine the effectiveness of this design.

The results of the tests with post layout data demonstrate that the proposed Analogue TDM scheme performs well even in the worst case scenario tested. With additional cable matching circuitry and with more realistic signal phasing as would be generated by a transducer array, the system should function with much lower channel crosstalk. Furthermore, the phase difference in the signals between channels in a narrow pitch ultrasound transducer would be much less than that which has been simulated meaning there would likely be a reduction in any crosstalk caused by adjacent channels as the voltage swing in the TDM signal between channels would be less.

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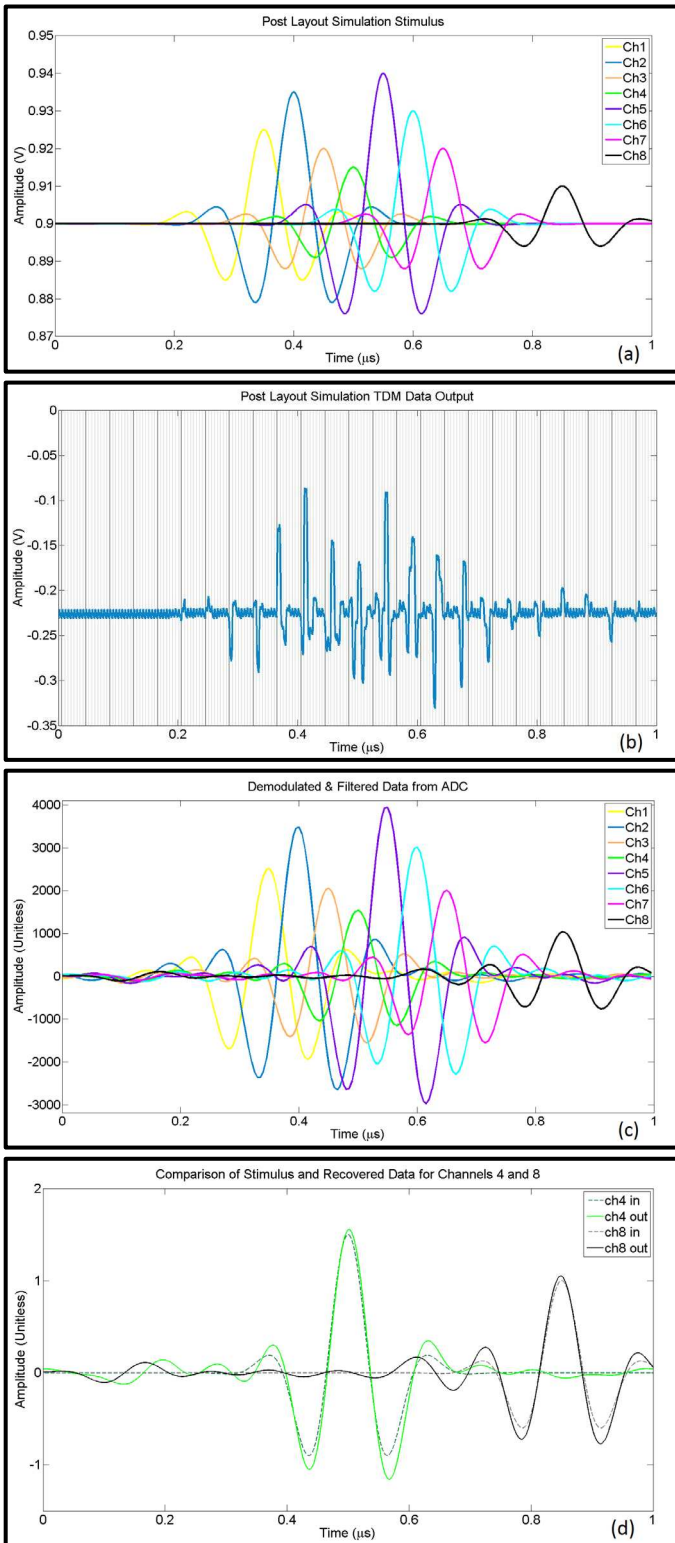
Fig. 5 (a) Input signals to post-layout simulation of TDM subsystem

(b) TDM Simulation output signal (major grid lines mark channel 1)

(c) Data captured by ADC then run through simulink demultiplexer

(d) Comparison of input and output signals (channels 4 and 8).