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# Thermal analysis of mid-infrared quantum-cascade lasers

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# ABSTRACT

We present a theoretical thermal analysis of mid-infrared quantum-cascade lasers (QCLs) using a two-dimensional anisotropic heat diffusion model. Several InP-based devices are simulated over a range of operating conditions in order to extract temperature-dependent thermal resistances. These thermal resistances are used to compare the effectiveness of various heat management techniques. Finally, heat flow analysis is performed in order to understand the internal thermal dynamics of these devices.

Keywords: quantum-cascade laser, mid-infrared, thermal modeling

#### **1. INTRODUCTION**

Mid-infrared (MIR) QCLs have shown a tremendous improvement in performance since their first demonstration.<sup>1</sup> High-power, above room-temperature (RT) continuous-wave (CW) operation is nowadays readily achieveable in InP-based devices.<sup>2–6</sup> Typically, QCLs suffer from large threshold currents and voltages meaning that significant amounts of electrical power are dissipated in the device active regions and converted directly to heat. This causes the active region temperature  $T_{\rm L}$  to rise considerably compared to the heat sink temperature  $T_{\rm H}$  which is detrimental to device performance through two main mechanisms (i) thermal backfilling of the lower laser level and (ii) thermionic emission from the upper laser level which combine to reduce the population inversion. In addition, the superlattice-like nature of QCL active regions is known to reduce both the in-plane ( $\kappa_{\parallel}$ ) and crossplane ( $\kappa_{\perp}$ ) components of the thermal conductivities compared to the bulk values of the constituent materials. This effect is caused by the layer widths being comparable to or less than the phonon mean free path which hinders the phonon transport,<sup>7,8</sup> reducing the efficiency of heat evacuation from the active region and further exacerbating the active region temperature rise.

Various attempts have been made with regards to improving the temperature performance of QCLs and these can generally be split into two approaches: (i) optimization of the quantum active region to reduce thermal backfilling and thermionic emission and (ii) the use of advanced thermal management techniques to improve the efficiency of heat removal from the active region. In this work we focus solely on approach (ii) and use a two-dimensional anisotropic model of heat diffusion in QCLs including temperaure-dependent material parameters to compare the thermal properties of different thermal management techniques. We use a standard ridge waveguide as a benchmark and compare it to a buried heterostructure (BH) device and a ridge wave guide with a thick electroplated (EP) gold top contact layer. A BH device<sup>9</sup> is one in which the device active region is completely embedded in semiconductor material, allowing heat flow from all sides of the active region. However, the improvement in temperature performance comes at the expense of the increased complexity of fabrication. Devices with thick EP gold top contact layers also allow heat flow to occur laterally from the active region but with the advantage of a much simpler processing technique.<sup>10</sup>

It is clear that in order to further extend the operating temperatures of MIR QCLs, knowledge of the internal thermal dynamics of the devices is mandatory. With this aim, in this work the above devices are simulated over a range of operating powers and temperature-dependant thermal resistances are extracted together with the power outflows from the device active regions. These parameters allow us to quantify the thermal properties of each device and help us to understand the internal thermal dynamics. In Sec. (2) we outline our thermal model and give the relevant material parameters. Sec. (3) presents a comparison of the temperature-dependent thermal resistances and finally we investigate the internal heat flows in Sec. (4) before drawing our conclusions.

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Figure 1. Five-point stencil used in the simulation. Temperatures are calculated at node P in the center of the cell defined by the dashed line. Each cell is of dimension  $\Delta x$  by  $\Delta y$ . Interface values of  $\kappa$  are denoted by the lower-case subscripts while nodal values have upper-case subscripts.

#### 2. THEORETICAL FRAMEWORK

In order to calculate the internal temperature profiles and hence the thermal resistances, an anisotropic thermal model of heat diffusion in QCLs is employed which is based upon Fourier's heat equation

$$\rho c_v \frac{\partial T}{\partial t} = \nabla \cdot [\kappa \nabla T] + Q \tag{1}$$

where  $\rho$  is the material density,  $c_v$  the specific heat capacity, T the temperature,  $\kappa$  the thermal conductivity tensor and Q the heat generated per unit volume defined by P/V where V is the volume of the active region.

## 2.1 Solution of the heat equation

In this work, we solve the two-dimensional heat equation in the steady-state (to represent CW operation) and hence Eqn. (1) is re-written as

$$\frac{\partial}{\partial x} \left( \kappa_x \frac{\partial T}{\partial x} \right) + \frac{\partial}{\partial y} \left( \kappa_y \frac{\partial T}{\partial y} \right) = -Q.$$
(2)

As in our previous work,<sup>11</sup> we solve Eqn. (2) using a finite-difference (FD) approach. The spatial domain where the solution is sought is discretized into a non-overlapping grid and Eqn. (2) is solved at the nodes with appropriate continuity of the solution across the interfaces between the nodes and subject to the relevant boundary conditions at the domain edge. Fig. (1) shows the five-point stencil used in the calculation.

Replacing the derivatives in Eqn. (2) with finite-differences gives

$$\frac{\kappa_e(T_E - T_P)}{\Delta x^2} - \frac{\kappa_w(T_P - T_W)}{\Delta x^2} + \frac{\kappa_n(T_N - T_P)}{\Delta y^2} - \frac{\kappa_s(T_P - T_S)}{\Delta y^2} = -Q_P \tag{3}$$

where the interface values of  $\kappa$  are denoted by lower-case subscripts and given by a harmonic mean of the appropriate nodal values such that the heat flux is conserved through the cell i.e.

$$\kappa_e = 2 \frac{\kappa_P \kappa_E}{\kappa_P + \kappa_E}.\tag{4}$$

In this work a uniform mesh of size  $\Delta x = \Delta y = 100$  nm is used in the simulations.

#### 2.1.1 Relaxation method

Nodal temperatures are calculated by re-arranging Eqn. (3) to make  $T_P$  the subject and solving using a relaxation method.

$$T_P = W \left[ (\kappa_w T_W + \kappa_e T_E) / \Delta x^2 + (\kappa_n T_N + \kappa_s T_S) / \Delta y^2 + Q_p \right]$$
(5)

where the weighting function W is given by

$$W = \frac{\Delta x^2 \Delta y^2}{(\kappa_w + \kappa_e) \Delta x^2 + (\kappa_n + \kappa_s) \Delta y^2}.$$
(6)

The temperatures of the nodes in the system are initialised to some arbitrary value (usually the heat sink temperature) and stepped through one-by-one in a sequential manner. At each point,  $T_P$  is updated following Eqn. (5) to give  $T'_P$  which satisfies the local FD equation. This process is repeated iteratively until the nodal temperatures converge to values that simultaneously satisfy all the FD equations. Convergence is defined by the maximum normalised residual in the system being below a pre-defined tolerance i.e.  $[T'_P - T_P]/T'_P < 10^{-6}$ .

It is possible to considerably speed up the convergence using a technique known as successive over-relaxation (SOR). Instead of applying the updated nodal temperature  $T'_P$ , an over-corrected value  $T''_P$  is applied.

$$T_P'' = \omega T_P' + (1 - \omega) T_P \tag{7}$$

where  $\omega$  is relaxation factor and can be in the range  $1 \leq \omega < 2$ . In this work a value of  $\omega = 1.7$  was found to give acceptable values of convergence while maintaining stability.

It is possible to take into account the temperature-dependent thermal conductivities of the materials in the device by updating the thermal conductivities using the current nodal temperatures after each iteration (Sec. (2.2) lists the thermal conductivities used in the simulations).

#### 2.1.2 Boundary conditions

The relaxation method as described in Sec. (2.1.1) is applied to all interior nodes in the system while at the exterior nodes it is necessary to apply the appropriate boundary conditions. For boundaries in contact with the heat sink, Dirichlet boundary conditions are applied and the temperature of boundary nodes are fixed at the heat sink temperature  $T_{\rm H}$ . For all other boundaries, no heat flow is assumed normal to the surface and hence Neumann ( $\nabla T(\mathbf{r}) = 0$ ) boundary conditions are utilized.

A Neumann boundary condition can also be used to take advantage of the symmetry of the structure. Since the structure is symmetric, the solution is also symmetric and therefore only needs to be calculated in one half of the structure with a Neumann boundary condition applied along the line of symmetry. This procedure reduces the memory requirements and increases the speed of convergence.

#### 2.2 Material parameters

In order to increase the accuracy of the model, temperature-dependent thermal conductivities are taken into account. The thermal conductivities of the materials used in the simulations are listed in Table (1). The data is taken from Ref. 12.

Material	$\kappa \; [\mathrm{W} \; \mathrm{m}^{-1} \; \mathrm{K}^{-1}]$
InP	$2.31 \times 10^5 T^{-1.45}$
InGaAs	$23 - 9.30 \times 10^{-2}T + 1.06 \times 10^{-4}T^2$
InAlAs	$20.5 - 8.40 \times 10^{-2}T + 0.95 \times 10^{-4}T^2$
Copper	349 + 14710/T
Gold	337 - T/15.15
Indium	$93.9 - 6.96 \times 10^{-2}T + 9.86 \times 10^{-5}T^2$
$SiO_2$	$0.0974 + 5.38 \times 10^{-3}T - 4.69 \times 10^{-6}T^2$

Table 1. Temperature-dependent thermal conductivities used in the simulations.

The cross-plane thermal conductivity of the active region is fixed at 2 W m<sup>-1</sup> K<sup>-1</sup> and the in-plane component is taken to be equal to 75% of the weighted average of the bulk constituents.<sup>12</sup>



Figure 2. (a) Temperature rise  $\Delta T$  as a function of electrical power P for: Device A - standard ridge waveguide, Device B - buried heterostructure and Device C - standard ridge covered in thick electroplated gold. Dashed lines are fits to Eqn. (8). (b) Intrinsic thermal resistance  $R_0$  as a function of  $T_{\rm H}$  for each device.

#### **3. COMPARISON OF DEVICE THERMAL PROPERTIES**

### 3.1 Device structures

In this work we investigate the thermal properties of three types of InP-based devices: a benchmark standard ridge waveguide (A), a buried heterostructure (B) and a ridge waveguide covered with thick EP gold top contact layer (C). In order to make comparisons between the devices more meaningful they have been kept as similar as possible and are based upon the device in Ref. 6. The active region is assumed to be 1.5  $\mu$ m thick with the well material (InGaAs) assumed to account for 63% of the total thickness. The upper cladding layer is formed by 3.5  $\mu$ m of InP and the InP substrate is assumed to be 100  $\mu$ m-thick. The laser ridge is assumed to have been etched to the bottom of the active region. A 250  $\mu$ m-thick copper heat sink and 10  $\mu$ m of indium solder are also included in the simulation. In all cases, the laser ridge is taken as being 12  $\mu$ m-wide and 3 mm-long. Device A is assumed to be covered in 300 nm of SiO<sub>2</sub> with an 8  $\mu$ m window for the 300 nm-thick gold top contact layer. The ridge in device B is assumed to be surrounded on both sides by i-InP and then covered in 300 nm of SiO<sub>2</sub> and 300 nm of gold (also with an 8  $\mu$ m window on top of the ridge). Device C is taken to be the same as A, apart from the 5.3  $\mu$ m-thick top gold contact layer.

The heat sink temperature is applied at the bottom of the copper heat sink and the active region is taken to be the only heat source (i.e. resistive heating in the cladding layers has been ignored). Due to the small wall-plug efficiencies of QCLs, the total input electrical power is assumed to be uniformly dissipated inside the active region volume ( $V = 1.5\mu m \times 12 \ \mu m \times 3 \ mm = 5.4 \times 10^{-14} \ m^3$ ).

#### 3.2 Thermal resistance extraction

By running simulations for a range of electrical powers, we can extract  $T_{\rm L}$  as a function of P for each of the three devices. We define  $T_{\rm L}$  as the temperature in the center of the QCL active region. The thermal resistance is then defined by  $R_{\rm TH} = dT_{\rm L}/dP$ . Fig. (2a) shows the temperature rise ( $\Delta T = T_{\rm L} - T_{\rm H}$ ) as a function of P for all three devices at  $T_{\rm H} = 300$  K. It can be seen that for all three devices, the temperature rise has a quasi-linear dependency for low powers and begins to deviate at higher powers. We have found the following empirical function to be an excellent fit to the data in Fig. (2a) with correlation coefficients in excess of 0.999.

$$\Delta T = T_0 [\exp(P/P_0) - 1].$$
(8)

Differentiating the above equation with respect to P gives an expression for the thermal resistance as a function of P

$$R_{\rm TH} = (T_0/P_0) \exp(P/P_0) = R_0 \exp(P/P_0)$$
(9)

where we define  $R_0$  as the intrinsic thermal resistance of the device. Fig. (2b) shows a plot of intrinsic thermal resistance  $(R_0)$  as a function of  $T_{\rm H}$  for each of the three devices. It can be seen from that figure that device A



Figure 3. Device thermal resistances as a function of electrical power at  $T_{\rm H} = 300$  K.

has the highest intrinsic thermal resistance for all values of  $T_{\rm H}$ . At heat sink temperatures below 165 K device B has the lowest  $R_0$  value while above this value, device C has the lowest.

By replacing the exponential function in Eqn. (8) with its Taylor series and neglecting the higher-order terms it can be seen that in the low power regime, Eqn. (8) recovers the form

$$\Delta T = R_0 P \tag{10}$$

which is often used in the literature.<sup>13, 14</sup> In this form the thermal resistance is constant irrespective of the change in the lattice temperature, whereas by combining Eqs. (8) and (9) we obtain a temperature dependent thermal resistance

$$R_{\rm TH} = R_0 \left(\frac{\Delta T}{T_0} + 1\right) \tag{11}$$

which takes into account the temperature-dependent thermal conductivities of the materials in the device. For values of P where  $\Delta T \ll T_0$ , then the  $R_{\rm TH}$  can be well approximated by  $R_0$  justifying the use of Eqn. (10), however for higher values of P when  $\Delta T$  becomes comparable to  $T_0$ , the quasi-linear relationship breaks down and a temperature-dependent  $R_{\rm TH}$  must be used. A plot of  $R_{\rm TH}$  as a function of P at  $T_{\rm H} = 300$  K for all three devices is shown in Fig. (3). At this value of  $T_{\rm H}$ , device A has the highest thermal resistance and device C the lowest, regardless of the value of P. It can be seen from the Figure that as P increases,  $R_{\rm TH}$  begins to significantly deviate from  $R_0$ , questioning the validity of the low power limit commonly used in Eqn. (10).

#### 4. HEAT-FLOW ANALYSIS

In order to understand the internal thermal dynamics of the devices, it is useful to know how the heat is evacuated from the active region. In this device the active region is cuboid in shape and the power which flows through each surface of the cuboid can be calculated as

$$P_f = \int -k(\mathbf{r})\nabla T(\mathbf{r}) \mathrm{d}\mathbf{S}$$
(12)

where in the steady-state the total power which flows through each surface is equal to the input electrical power P dissipated in the active region volume. Here we have neglected power flow through the front and back facets of the active region. The calculated power outflow through each surface of the active region (out of the top through the upper cladding, laterally, and through the bottom into the substrate) for P = 5 W at  $T_{\rm H} = 300$  K for each device is shown in Table (2).

It can be seen from the table that with respect to device A, the majority (68 %) of the heat dissipated in the active region escapes through the substrate. The extra 5  $\mu$ m of gold in the case of device C compared to device A increases the amount of heat escaping through the top of the active region by ~ 70%, causing a subsequent reduction in the amount escaping through the substrate to ~ 50% of the total. In device B (the BH),

Table 2. Total amount of heat flowing through each surface calculated as a percentage of the total input electrical power (5 W) at  $T_{\rm H} = 300$  K for each device.



Figure 4. Power outflow for device B as a function of  $T_{\rm H}$  at P = 5 W showing the percentage of heat escaping through each surface of the active region.

the lateral heat channels are enhanced by  $\sim 60\%$  compared to device A; taking advantage of the higher in-plane thermal conductivity of the active region compared to the severely reduced cross-plane conductivity. Although increasing the lateral heat escape channels reduces the active region temperature, there is a limit on how much these channels can be enhanced which is determined by the aspect ratio of the active region. In this particular case, the active region has an aspect ratio of 8:1, meaning that vertical heat transport will always dominate over lateral heat transport. Reducing the laser ridge width will reduce the aspect ratio and increase the effect of the lateral heat channels on the active region temperature.

Fig. (4) shows a plot of the power outflow through each surface of device B as a function of  $T_{\rm H}$  for P = 5 W. It can be seen from the figure that as  $T_{\rm H}$  is increased, there is a suppression of the lateral heat escape channels - likely caused by the reduction of the in-plane thermal conductivity of the active region with temperature - and this probably explains the crossover of the curves for devices B and C in Fig. (2b). As the fraction of heat that escapes through the substrate remains approximately constant, the suppression of the lateral heat escape channels is compensated by an increase in the amount of heat that escapes through the upper cladding layer. This heat that evacuates the active region via the upper cladding layer then streams towards the heat sink through the i-InP surrounding the laser ridge.

The effect of varying the thickness of the gold layer of device C on the lattice temperature and the heat outflow components is shown in Fig. (5) for P = 5 W at  $T_{\rm H} = 300$  K. As the thickness of the gold layer increases, the lattice temperature steadily drops. By comparing the data for device B in Fig. (2) with the above figure, it can be seen that at  $T_{\rm H} = 300$  K, the critical thickness of the gold layer is ~1.5  $\mu$ m. For thicknesses above this value, the rise in temperature is less in device C than for device B. It should be stressed that this critical thickness is not universal, it can be expected to change with  $T_{\rm H}$  and the ridge aspect ratio.

Fig. (5) also shows that the amount of heat that escapes laterally is almost independent of the thickness of the gold layer. Instead, as the gold layer thickness increases, the fraction of heat that escapes through the upper cladding increases and offsets the decrease in the fraction of heat that escapes through the substrate. As the layer becomes even thicker, the fractions of heat escaping through the vertical channels begin to balance, indicating that the high thermal conductivity gold layer begins to act as a pseudo heat sink.



Figure 5. Power outflow for device C as a function of gold thickness d for P = 5 W at  $T_{\rm H} = 300$  K showing the percentage of heat escaping through each surface of the active region. Also shown is the lattice temperature  $T_{\rm L}$  as a function of d.

#### 5. CONCLUSIONS

We have presented a thermal analysis of mid-infrared InP-based QCLs using a two-dimensional steady-state anisotropic heat diffusion model which takes into account temperature-dependent material properties and the reduced thermal conductivity of the superlattice-like active region in the direction perpendicular to the layers. The heat equation is solved using finite-differences and a successive over-relaxation technique.

We have introduced an empirical expression for a temperature-dependent thermal resistance which arises through non-constant material thermal conductivities with regards to lattice temperature. It has been shown that in the limit of low dissipated electrical power, the thermal resistance can be assumed to be constant, however as the dissipated power is increased, significant deviation can be expected. In all cases the benchmark standard ridge waveguide is found to perform the worst with the highest values of thermal resistance. At P = 0 W,  $R_{\rm TH} \sim 12$  K/W and increases to  $\sim 19.5$  K/W at P = 10 W. For heat sink temperatures of less than  $\sim 165$  K, the intrinsic thermal resistance of the EP gold device is higher than that of the BH and above this temperature the situation is vice versa.

We have also carried out heat flow analysis on each device. Due to the lack of lateral heat escape channels in the benchmark ridge structure, the majority of heat streams from the active region via the substrate. When the active region is encapsulated in semiconductor material as in the case of the BH, the lateral heat channels become more efficient and allow more heat to escape both directly and indirectly (via the upper cladding layer) into the surrounding semiconductor, causing a reduction in the thermal resistance of the device. For the case of the device with a thick EP gold contact layer, approximately half of the heat escapes via the substrate as in the case of the benchmark ridge, while the majority of the remaining heat escapes via the thick gold layer with the lateral heat channels playing only a minor role. We have found that as the heat sink temperature is increased, the lateral heat escape channels in the BH are suppressed as a result of a reduction in the thermal conductivity of the surrounding semiconductor layers and cause the cross-over in intrinsic thermal resistance with the EP gold device as mentioned above.

With regards to the EP gold device, we have investigated the effect of the gold layer thickness on the heat flow behavior at room temperature. For all thicknesses, the lateral heat flows are approximately constant and as the thickness increases, the fractions of heat that escapes via the gold and the substrate begin to balance, suggesting the gold is acting as some sort of pseudo heat sink. We have found that the critical thickness (where the thermal resistance of the EP gold device is lower than the BH device) of the gold in this particular case is  $1.5 \ \mu$ m, although this will depend heavily on the heat sink temperature and ridge aspect ratio.

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