Immunity of FPGA Chips by Direct Injection

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***Abstract* — Immunity measurements of Xilinix XC3S200TQ144 and Altera EP3C10E144C7N FPGAs by direct injection are presented and the immunity of individual pins is shown to depend greatly on the load seen by nearby pins. The implications of this on in-circuit immunity prediction are discussed.**

1. INTRODUCTION

To allow the immunity prediction of whole electronic systems a characterisation of the individual components used within is required. When working towards a predictable system we initially choose a Xilinx XC3S200TQ144 FPGA to be the ”heart” of the system. After performing initial measurements with the IC-Strip line method [1] we found that the FPGA appeared to be fairly immune to the field levels we could apply to it. To increase the RF pick-up we started attaching tracks to the IC. Measurements then showed - as assumed - that the susceptibility increased. Doing further measurements it showed that using different terminations at the end of the tacks attached to the FPGA made significant differences to the immunity of the IC which could possibly be explained using transmission line theory. Surprisingly it was also found that changes on pins which were not monitored made a difference to the immunity of monitored pins. To separate the effect of the pickup on the tracks from the immunity of the IC direct injection (DI) measurements were carried out.

2. EXPERIMENTAL RESULTS FOR XILINX FPGA

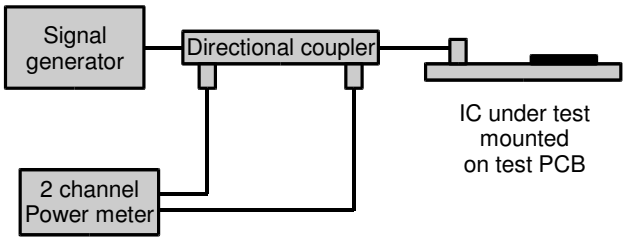

Fig. 1 Experimental setup for direct injection immunity tests. In some cases a power amplifier is inserted after the signal generator.

The immunity tests were performed by injecting a continuous wave signal into the pin under test and monitoring at which power level it "failed" following approximately the method of IEC 62132-4 [2]. As all input pins were pulled down with internal pull-down resistors a failure was defined as a "high" being detected when polling the pin. The FPGA was programmed to hold a MicroBlaze processor [3] that was configured to poll an input pin under test and to communicate the pin status to a PC using a UART connection. Earlier tests showed that the input logic failed before the core did. This can also be seen by the fact that the MicroBlaze processor is still able to receive commands and return the status when the input pins are detected as high. If the FPGA core would fail first, the MicroBlaze would not be able to receive commands or react to them in a proper manner. The I/O buffers were operated in the default 2.5 V configuration during the following measurements (but powered with 3.3V). However changes to the configuration did not affect the susceptibility of the IC.

2.1 The effect of adjacent pin loading

The first experiment conducted was to measure the immunity of P59 with all other pads being left open. They were only internally connected to ground using the pull-down resistors. Figure 3 shows the immunity data

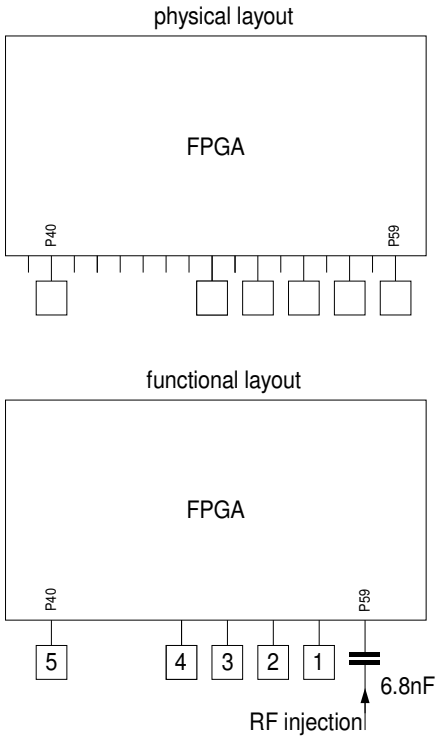

Fig. 2 Physical and Functional Layout of IC pins used for direct injection.

for P59 including signal generator output power, forward power, reverse power and the injected power calculated from forward and reverse power.

Since we then knew the immunity of P59 in the "undisturbed" case we started to measure the effect of the termination of the adjacent pins / pads. As we had some significant effects with stripline measurements when

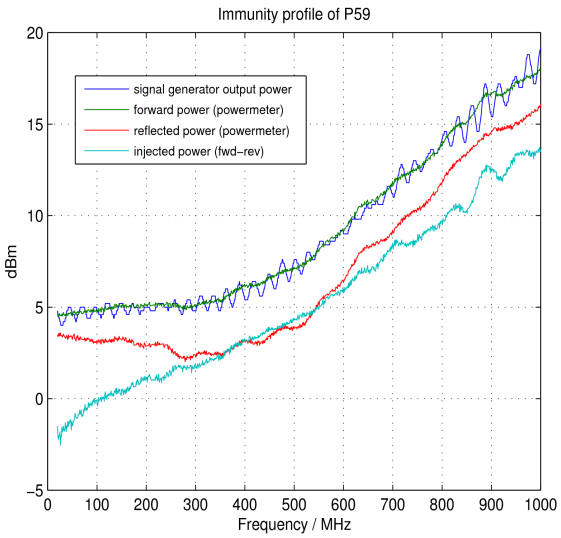

Fig. 3 Immunity of P59 with adjacent pins open (internal pull-down).

pins, which were open in the first instance, were connected to ground with 100pF, it was decided to move a 100pF connection to ground from Pad 2 to Pad 5 and see how it effects the immunity of P59. Figure 4 shows the injected, forward, and reverse power needed to fail P59 depending on the position of the 100 pF grounding capacitor.

Analysing these measurements brings up 3 things.

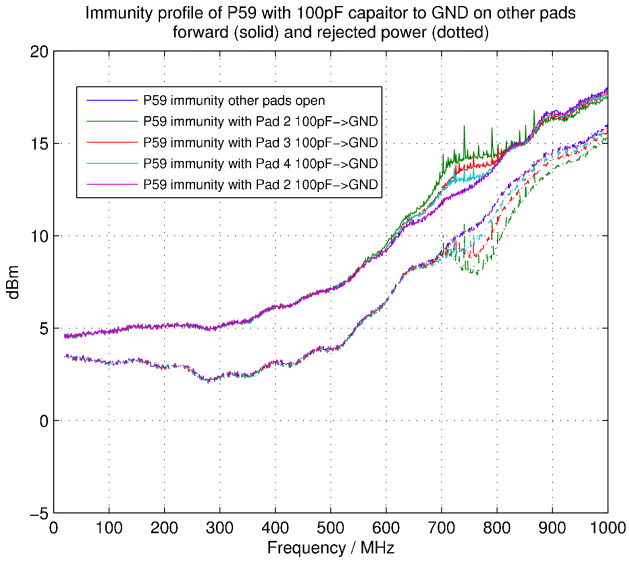

Fig. 4: Immunity of P59 showing the effect of connecting P1 to P5 to ground via 100 pF capacitor

Firstly, connecting a 100pF capacitor to the pads appears to increase the immunity of P59 for a frequency range somewhere between 600 and 900 MHz. It can also be observed that this effect becomes smaller as the physical distance (pin distance) from the 100pF grounding capacitor to the injection pin increases. Secondly, looking at Figure 4 it appears that when more power is required to fail the IC (bigger forward power) the rejected power

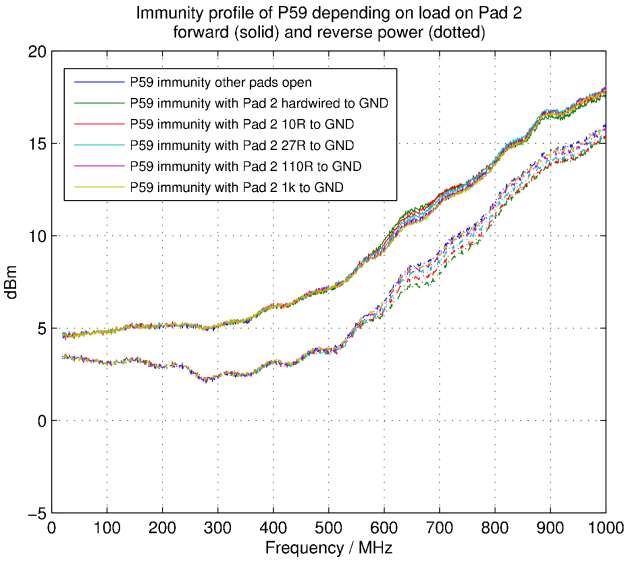

Fig. 5: Immunity of P59 with Pad 2 connected to different grounding resistors (forward and reverse power)

becomes smaller. On the first sight this might be surprising as one would assume that the reflected power would also go up or remain at least constant as more power is required to fail the pin. However it appears the the increased power also drives the protective clamping diodes further into conduction and hence more power is dissipated that way rather than being reflected. It could also be the case that due to more voltage injected into the pin the diodes become more conductive and hence the pins' input impedance better matches the track impedance which also results in less reflected power. Thirdly, when the 100pF grounding capacitor is connected to Pad 5 the effect of increased immunity is practically gone. To ensure that the effect was also not caused by the value of the capacitor Pad 2 was also grounded by using a 470pF capacitor as a change in resonance frequency could be observed if the capacitor value was the origin of it. There was no significant change in the behaviour observed.

After this measurement resistive terminations were used at Pad 2 to evaluate the effect of grounding resistors rather than capacitors which might have been a reason for this resonance like behaviour. Figure 5 shows the results of the terminating resistor measurements. It can be seen that also for the resistive terminations the effect of increased immunity occurs. It appears the the higher the resistance the lower the effect becomes. It can also be observed that the frequency range of the effect appears to be the same as before (apart from minor shifts in the peak frequency).

Figure 6 compares the "worst" resistive termination with both 100pF, 470pF grounding capacitors and the "undisturbed" case. It can be seen in Figure 6 that the change in the capacitance value by a factor of roughly 2.3 does not significantly affect the immunity "resonance". This implies that this "resonance" frequency is not due to the external components connected. Up to this point it can be concluded that the effect of increased immunity is depending on the distance of the "ground path".

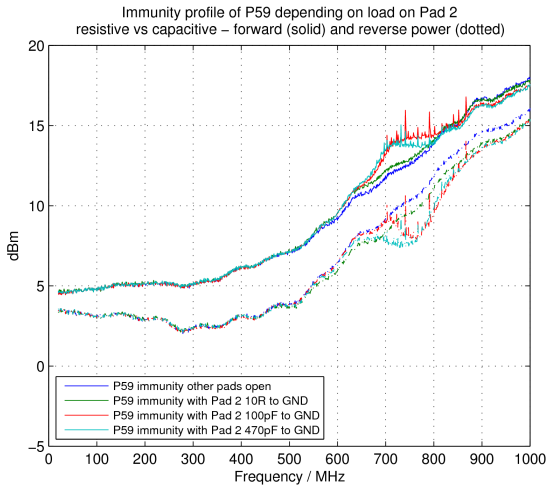

Fig. 6: Comparison of P59 immunity depending on Pad 2 terminations "worst case" comparison.

To confirm what we measured for P59 and to get an idea of the immunity variation between the different pins we measured the immunity of P40. This was the only pin that could be used due to physical constraints on the board. We measured both the "undisturbed" case (all other pads open) as well as cases where some of the pads were grounded with 100pF or similar. Before this we confirmed that mounting the extra track to P40 did not affect the immunity of P59. It was not assumed to do so

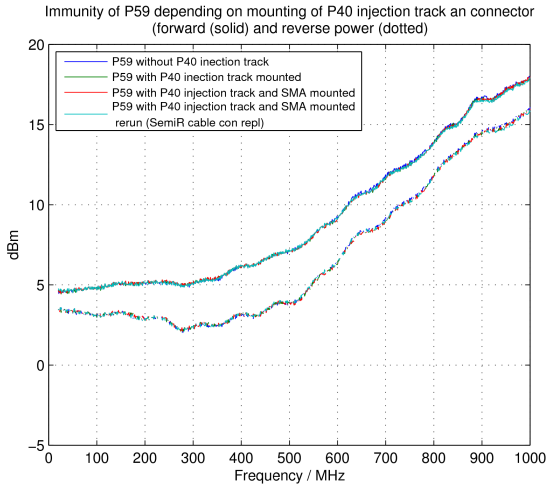

Fig. 7: P59 immunity depending of the presence of P40 injection track and connector.

as above measurements showed that changes in the termination on Pad 5 (equal to P40) did not affect the immunity of P59. Figure 8 confirms this expectation for both the undisturbed case as well as for the case when Pad 4 is connected to ground with a 100pF capacitor.
The next step was to measure the immunity of P40 in the "undisturbed" case and to compare it with the one of P59. This gave us an idea of the immunity variation between the pins. The results are shown in Figure 7.
We then tried to verify the effect that a capacitor at one of the other pads would affect the immunity of P40. The pad closest to P40 was Pad 4 which was expected to give

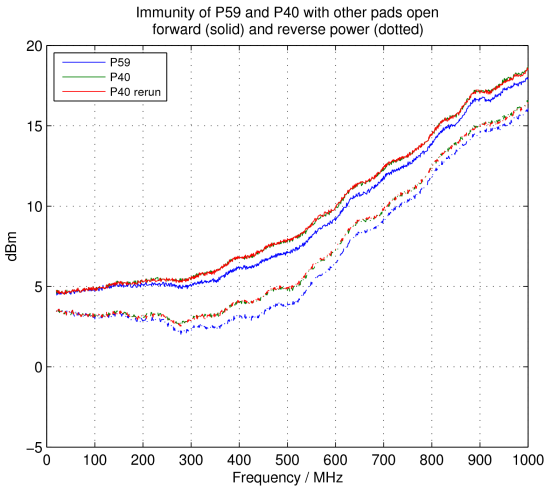

Fig. 8: comparing the immunity of P40 and P59 for the "undisturbed" case.

a similar curve as P59 with a 100pF load at Pad 3 or Pad 4. Figure 9 compares the immunity of P40 between the undisturbed case and the case when Pad 4 is connected to ground with a 100pF capacitor. It can be observed that the presence of the capacitor at P40 does not seem to have any significant effect on the immunity of P40. Comparing this to the behaviour of P59 it appears that P40 is more immune to termination changes of the other pads than P59. To find a reason for this we had a look at the layout of the chip. We found that between P59 and

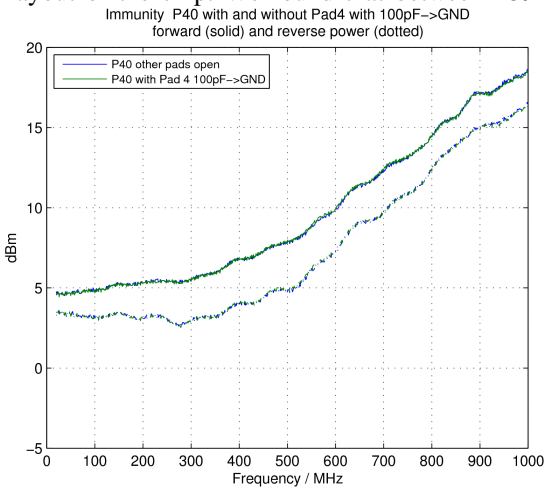

Fig. 9: P40 immunity comparing undisturbed case with Pad 4 with 100pF to GND case.

Pad 4 no ground pin was present but that there were 2 ground pins between Pad 4 and Pad 5. Taking into account the facts that a capacitor at Pad 5 (equal to P40) had no effect on the immunity of P59, that mounting the SMA connector onto P40 had no effect on the immunity of P59 either and that a grounding capacitor on Pad 4 has no effect on the immunity of P40 we assumed that the ground pins have a shielding effect.

2.2 The effect of alternate pin grounding

In an endeavour to isolate the effect of coupling between nearby pins and their loads on the immunity of an

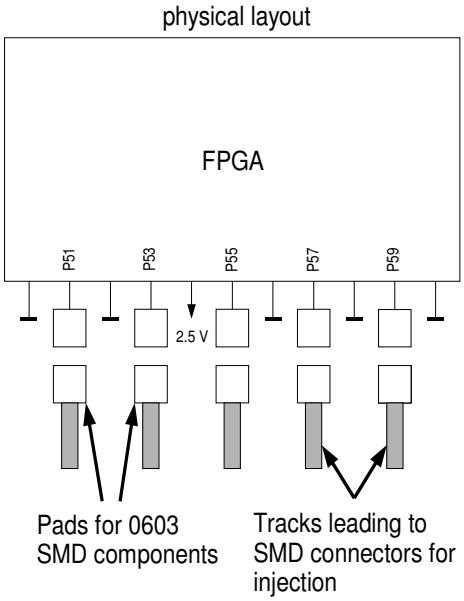

Fig. 10: Redesigned board layout with every other pin connected to ground (where possible)

individual pin we developed a board where alternate pins were grounded. The concept is shown in Figure 8. Figure shows the effect of connecting a 100 pF termination to nearby pins on the new board. Figure 11 shows that the effect of the changing termination is reduced compared to the case where intermediate pins were not grounded.

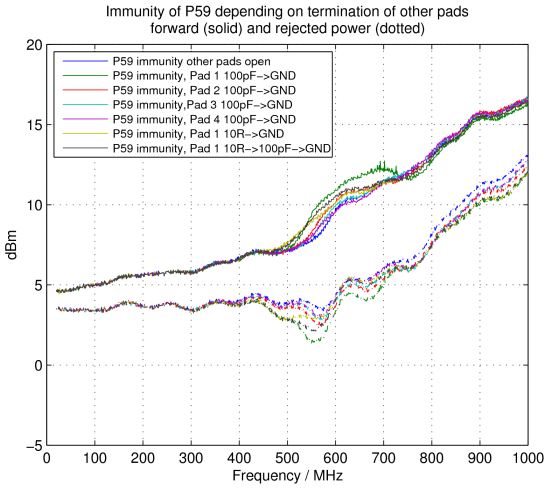

Fig. 11: P59 immunity depending on presence of grounding at Pads 1 to 4 (injected power)

We also observed that the configuration of the grounded IO pin affected the immunity of nearby pins

2.3 On-chip coupling between pins

The above measurements implied that the change in immunity was due to both the presence of injection tracks as well as on chip cross coupling between the pins. It was hence decided to get an idea of the coupling between the individual pins by measuring the S-Parameters between the individual feeding connectors. Figure 12 shows the

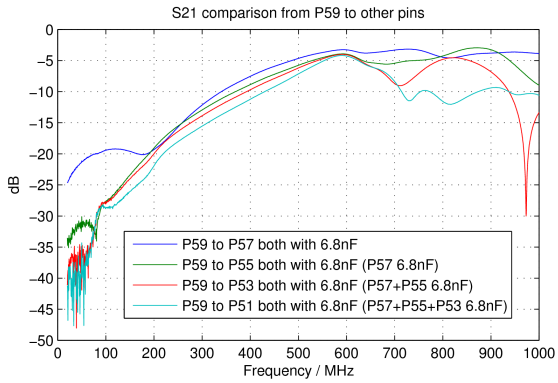

Fig. 12: Pin 59 coupling to nearby pins

coupling measured between pairs of nearby pins. It can be seen that strong coupling can occur above 400 MHz. We further investigated the track to track coupling and lead-frame coupling of the device and established that the coupling seen in Figure 12 is dominated by on-chip effects.

3. EXPERIMENTAL RESULTS FOR ALTERA FPGA

In order to gain further insight as to whether the effects observed with the Xilinx FPGA were generic or particular to that device, an comparable Altera device was examined. Provision was made to access a larger number of IO pins so that a comparison of pin-to-pin

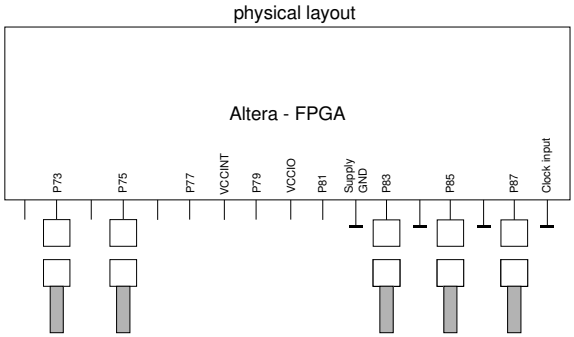

Fig. 13: Altera FPGA pin layout for direct injection immunity tests.

variations could be made.

3.1 Immunity variation between pins

Figure 14 shows the immunity variation between the Pins 87, 85, 83, 75 and 73. It can be observed that the immunity profiles follow a common trend but that the variation between them can be as big as 5 dB in excess. One could try to argue that that the grounded pins 84 and 86 together with the clock input P88 that is unused and hence also grounded improve the immunity of the pins 87 and 85. However pin 82 is a power supply ground pin which could (should?) in theory have the same effect but pin 83 is significantly less immune than both pin 87 and 85. One can only speculate that grounding I/O and clock

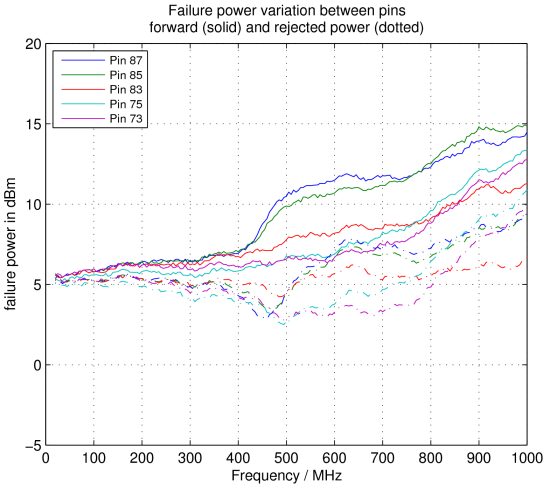

Fig. 14: Immunity variation between the different Pins

pins does improve the immunity of adjacent but a power supply pin does not - which is rather far fetched. However the grounding of adjacent pins seems to have at least some effect.

3.2 Effect of adjacent pin loading on immunity

Figure 15 shows the change in immunity of pin 85 when adjacent pins are left open compared to when injection

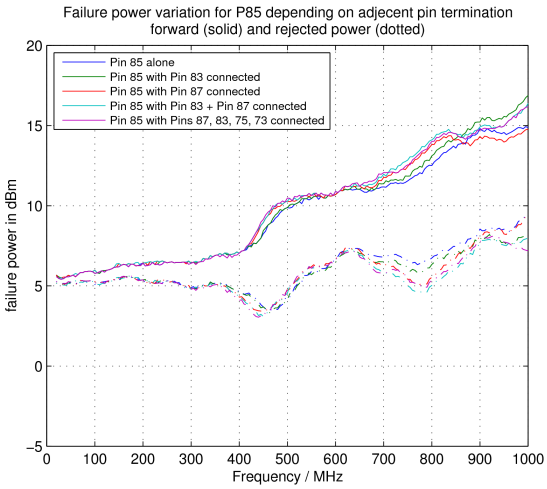

Fig. 15: Immunity variation of Pin 85 depending on connection of other pins to their feeding tracks

tracks are connected via a 6.8nF capacitor.
Figure 16 shows the effect of differing termination of adjacent pins on the immunity profile of pin 75.
Analysing the results it can be seen that pin 85 which is located between grounded I/O pins appears to be less susceptible to changes on its neighbour pins than pin 75 whose neighbours are left floating. The immunity of Pin 75 is strongly affected by the termination of Pin 73 which supports the theory that on chip coupling occurs. As for both the Altera and the Xilinx FPGA the resonances where at similar frequencies we wondered whether the effect we measure is actually due to the chip or the

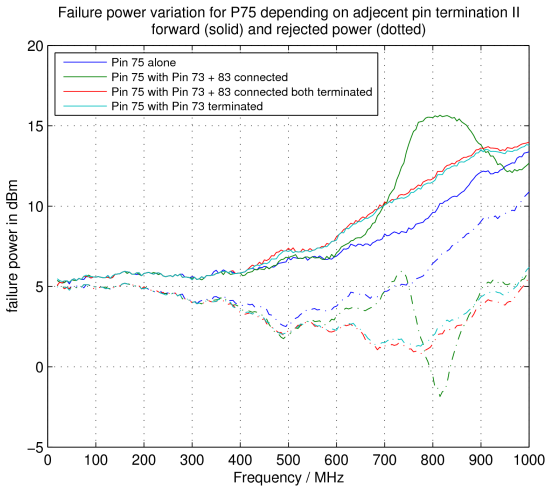

Fig. 16: Immunity variation of Pin 75 depending on connection of other pins to their feeding tracks

feeding capacitors. Performing measurements to determine the self resonance frequency of the 6.8nF X7R 0603 capacitor showed that the resonance is at about 46 MHz. This lines up with the manufacturers information which states the self resonance frequency to be 47 MHz. As the resonance peak in the immunity is at about 800 MHz the capacitor can be ruled out to be responsible for this.

4. CONCLUSION

In terms of forward power variations of 3-4 dB occur in the immunity of an individual pin dependent upon the load connected to adjacent pins and their IO configuration. In some cases resonant effects can considerably increase the discrepancy in measured immunity of a pin, depending on the load present on adjacent pins. The strong interaction between pins was also observed in direct coupling measurements between nearby pins.
We observed comparable immunity levels in the two device types examined and saw comparable interactions between pins. We have also observed similar on-chip pin-to-pin coupling effects at high frequencies in op-amp integrated circuits.
The variation of immunity of any pin with the load connected to adjacent pins complicates the problem of immunity analysis and prediction for realistically complex circuits.

5. REFERENCES

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