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Applying IEC 62132-2 to the real world: Immunity of an analogue to digital converter

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***Abstract*—The susceptibility of an analogue to digital (A/D) converter was measured according to IEC 62132-2 (TEM cell). The chip on its own had a high immunity as the lead-frame presents a small loop area and picks up little energy from an interfering source. With a small (15mm) track added the immunity was greatly reduced and showed a number that the interference had least effect at harmonics of the A/D converter clock frequency.**

***Keywords*—IC immunity, IEC 62132, TEM cell**

I. Introduction

This paper describes the some results of our work to enable the prediction of the immunity of electronic systems to radiated emissions. In order to be able to predict the immunity of a whole electronic system, it is crucial to know the immunity of the individual components. We performed our measurements according to the recently released standard IEC 62132-2 [1] which exposes the IC under tests to the RF disturbance source by using a TEM-cell. As we were aware that ICs have very small physical dimension which could work as a receiving antenna for the RF we decided to start our test series with an 12-Bit A/D converter [3] with an analogue bandwidth of 750 MHz which we believed would be more sensitive to RF disturbance than typical digital logic devices. The paper first describes our test setup, then show results when the A/D converter is measured without tracks attached to it, explain the problems with this and then compare these results with data obtained when a 15 mm track is attached to the A/D converters input. We will furthermore show, that an analysis of the histogram's shape around the undisturbed value will allow us to decide if the A/D converter sampled at random points of the continuous wave interference. We will also point out some interesting effects of the disturbance frequency in relation to the clock frequency.

II. Experimental Setup

When performing measurements according to IEC 62132-2 a 100×100 mm test PCB is recommended in the standard. This PCB accommodates the IC under test on one side and all supplementary components on the other side. The PCB is then mounted on an aperture in the TEM-cell housing with the IC under test facing inwards (Figure 1). This setup allows only the IC under test to be exposed to the interfering signal, while all supplementary components are shielded and hence assumed to be undisturbed. The IC under test is then exposed to RF which was in our case generated by a signal generator and then amplified by a power amplifier with an output power of about 30 W at mid band. This signal was then injected into one port of the TEM cell whilst the other was terminated by a 50 Ω high power load. In our test system the supplementary components are also shielded by an enclosure to ensure that no other external noise could possibly affect the measurement results. The enclosure also accommodates optical transmitters and receivers to allow communication between the device under test and an external monitoring system which was in our case a PC. This arrangement allows us to illuminate the IC in other environments such as a reverberation chamber.

In the contrary to the standard requirement's our test setup only allowed us to have a test PCB of approx. 60×60mm which is due to restraints of existing equipment but still believed to be sufficiently large enough to gain sensible results.

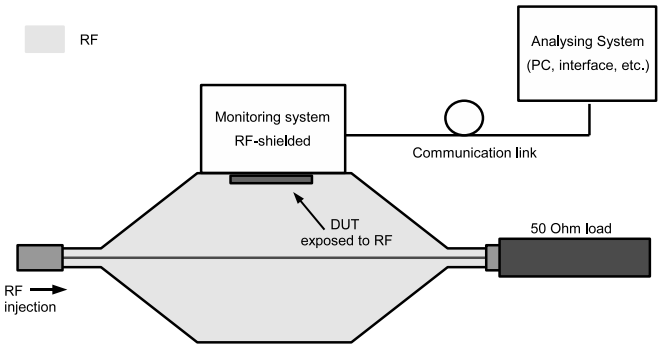

Figure 1. The test setup

III. Measurements, Results and Analysis

Firstly we measured the A/D converter in the frequency range between 200 MHz and 1 GHz with frequency steps of 10 MHz as specified in the standard [1]. As it can be seen in Figure 2, the A/D converter is hardly affected by the RFI. Nearly all the samples taken have the value of

the undisturbed A/D converter value which is somewhere between 2049 and 2051. It can be seen that the peak is a bid ”widened” due to the A/D converter capturing the interference magnitude –this effect will be explained later on.

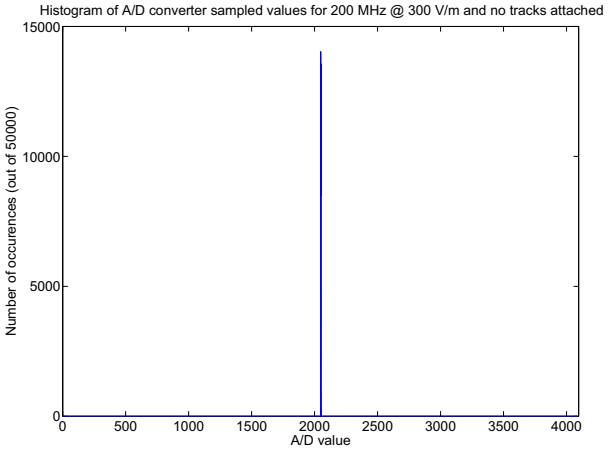

Figure 2. Histogram of ADC values for 300 V/m cw interference at 200 MHz with no tracks attached

We found the IC was fairly immune up to 350 V/m, the maximum available from our system. However as we know that once it is on a circuit board with tracks, more energy will be induced into the IC pins for a given interference level. One could argue what another way of getting more energy into the IC would have been to use an IC-Strip line which allows to generate high field strengths with low power levels [2] and leaves the IC in the setup as defined by the standard. However, we think that measuring an IC with tracks attached is far closer to reality. Apart from very sophisticated designs - were all the tracks leading to the IC are buried in the internal layers of the PCB - most devices have tracks leading to the IC and hence act as antennas. Measuring an IC without tracks attached is of course a well defined and reproducible state but it is not comparable with installation in a real system. We therefore added a 15 mm long track with a width of 1mm to one of the A/D converters differential inputs to increase the sensitivity of the immunity measurement.

With this new configuration we repeated the measurements from above. It can be seen from the results shown in Figure 3 that a level of 50 V/m is enough to produce errors. It can be observed that there is a maximum around the undisturbed A/D converter output value of 2050 and various smaller peaks at different values on the histogram. When looking at these results we were sure that the minor peaks were errors due to the RF exposure, but we also noticed that the middle peak was wider than before. Figure 4 shows a magnified view of this middle peak along with the theoretical distribution for a sinusoidal signal.

The fact that there were now 2 peaks with neither of

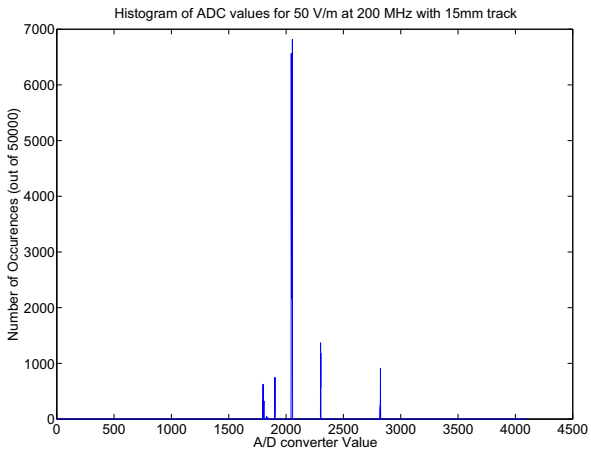

Figure 3. Histogram of ADC values for 50 V/m cw interference at 200 MHz with a 15mm track on one A/D converter input

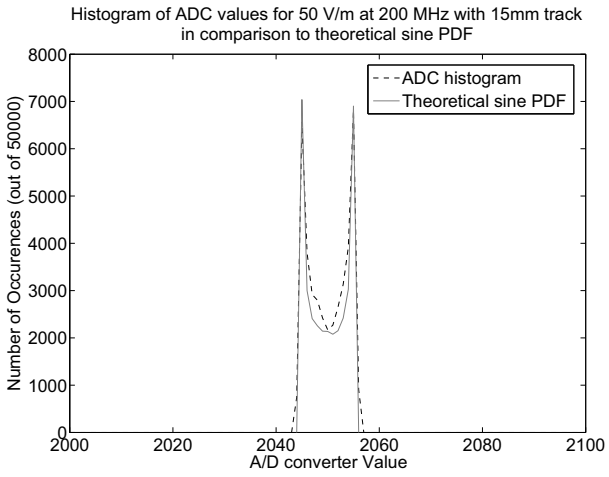

Figure 4. Histogram of ADC output values for 50 V/m cw interference at 200 MHz with a 15mm track on one A/D converter input compared with the theoretical sine-wave PDF

them being at 2050 or near it caused confusion in the first instance. However we found that this shape contains quite valuable information. To understand this it has to be explained that an A/D converter with no errors occurring would simply sample its input signal. Looking from a slightly different point of view the system we build is nothing but an A/D converter that samples the signal received by the 15 mm track that acts as an antenna. Knowing that the noise signal was sinusoidal, the middle peak's shape makes perfect sense as it is nothing else than the probability density function (PDF) sinusoidal interfering signal. The PDF $p(x)$ of a sine wave with unit amplitude can be described by the following equation:

$$p(x) = \begin{cases} \frac{1}{\pi\sqrt{1-x^2}} & \text{for } |x| < 1 \\ 0 & \text{otherwise} \end{cases} \quad (1)$$

which is obtained by differentiating the inverse sine function, and normalising so the the pdf has unit area [4]. Even

though the A/D converter runs at a clock frequency of approx 2.5 MHz it samples the sinusoidal interference signal perfectly well as it has an analogue input bandwidth of 750 MHz. The interfering signal is of course undersampled and the A/D converter samples randomly at any point of the interfering sine wave as the phase of the sample clock and interfering signal are not locked. This contains two pieces of information: If the A/D converter's clock signal and the interference frequency were locked in any way the A/D converter would always sample at the same point of the interfering sine wave. As the shape of the histogram around the undisturbed value is close to the theoretical PDF of a sinusoidal signal it is likely that the clock frequency and the interference frequency are not phase locked and that the samples are taken at random points of the interference signal. Secondly we can use the known pdf to define a measure for any errors induced in the A/D converter by the interference. We know that the shape of the pdf in the middle is that of a sampled sine wave and assume that all values inside this shape are correct samples whilst for all samples outside the A/D converter must have been affected by the RFI.

Figure 5 shows how the width of the sine PDF evolves with increasing frequency at a fixed level of 300 V/m. It can be observed that with rising frequency the sine PDF becomes wider - which makes sense as the 15mm track becomes a more efficient antenna increasing the level of the interference at the A/D input.

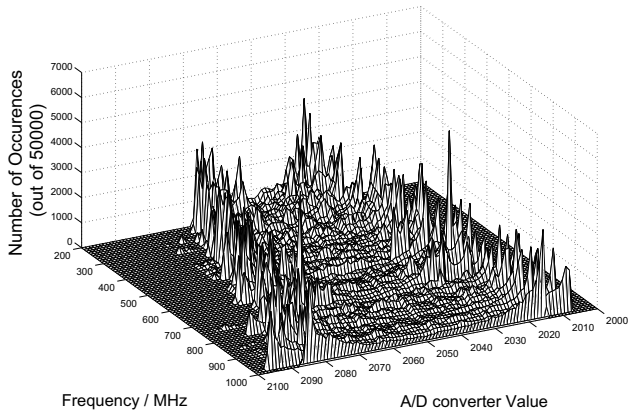

Figure 5. Histogram of ADC values for 50 V/m cw interference at 200 MHz with a 15mm track on one A/D converter input

The results above allowed us to formulate a measure for the immunity of the A/D converter. Looking at Figure 5 shows that the histogram for the centre PDF ranges over the values 2000 to 2100, ignoring minor excursions outside the PDF for lower frequencies. This range is now assumed to contain all the samples which are not in error meaning all the samples outside this range are considered to be in error. We then calculated the percentage of samples outside the middle range of proper operation with regard to the number of overall samples:

$$e = 100 - \frac{\sum_{n=2000}^{n=2100} p(n)}{\sum_{n=1}^{n=4096} p(n)} * 100$$

where n is the histogram bin, $p(n)$ is the value stored in that bin and e is the percentage of samples outside the sine PDF.

Using this measure it is possible to plot a graph that shows the error as a function of frequency and field strength. This is shown in Figure 6 where the the proportion of samples in error, e, was measured at 10 MHz intervals according to IEC 62132-2 [1] and the field strength increased in steps of 10 V/m .

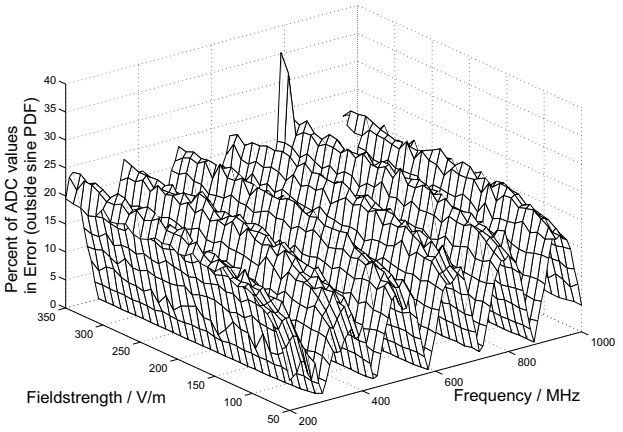

Figure 6. Histogram of ADC error rates for 50 V/m cw interference with 10 MHz frequency steps and with a 15mm track on one A/D converter input

The pattern observed poses 2 questions: Why does the error seem to saturate above 120 V/m even if the field strength is increased? Secondly why does the error change with frequency in a periodic manner? The answer to the first question is: we don't know - this certainly requires further investigation. The answer to the second question required a more detailed investigation. Due to the periodic character of the minima we assumed a standing wave problem. After checking our calibration data and re-measuring all S11 parameters we were able to say that there is certainly not a standing wave problem. As the frequency steps of 10 MHz were quite wide, we decided to remeasure the proportion of samples in error over the frequency range between 200 MHz and 1 GHz in steps of 1 MHz. The results obtained from these measurements were still not satisfactory as this produced another, different periodic variation in the error rate which suggested that we were still undersampling the phenomenon. We finally decided to measure the first 20 MHz with frequency steps of 10 kHz. The results are shown in Figure 7.

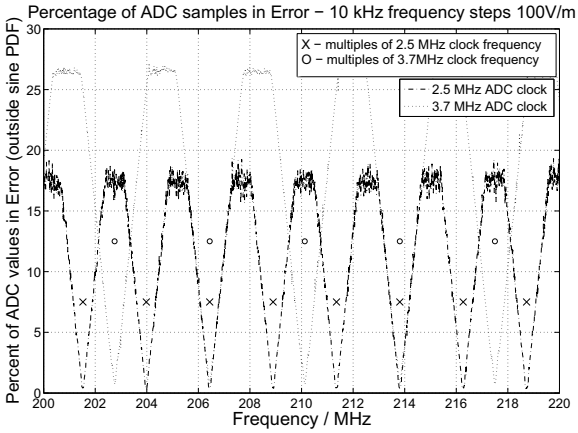

Figure 7. Histogram of ADC error rate for cw interference of 50 V/m over the range 200-220 MHz in 10 kHz steps with a 15mm track on A/D converter input and with sample clocks of 2.5 and 3.7 MHz

It can be seen that the error seems to be constant over a part of the frequency range, then drops almost linearly with frequency to a minimum, and rises again in a similar manner. This behaviour repeats periodically. Looking at the multiples of the A/D converter clock, it can be found that these are actually located at the minima of the errors (represented by an X in the figure). Hoping to gain more information we changed the A/D converter clock frequency to approximately 3.7 MHz and repeated the measurement. The result can also be found in Figure 7 where the frequency multiples for the 3.7 MHz A/D converter clock are indicated by a circle. When comparing both plots it is surprising that the error rate saturates at a certain level and and has a minimum when the interfering signal is near a harmonic of the sample clock. It is also noticeable that the slope from the minima upwards seem to be the same for both clock frequencies. We were surprised to see this effect as the disturbance signal was about 100 times higher (200 MHz to 1 GHz) than the A/D converter's clock signal (2.5 MHz and 3.7 MHz). Looking for the reason for the above behaviour we suspected that the clock frequency might be pulled by the external noise signal so that the sample rate and interference were phase locked when the interference was near a clock harmonic. Measuring the clock showed that this was not the case. We still do not understand what exactly happened there and will investigate this in the future.

IV. CONCLUSION

We have shown how we applied the current standard for TEM-Cell immunity measurements to a real world's problem. It is known that the TEM-Cell is not an ideal method to measure ICs as the field strengths which can be obtained are comparably low with regard to methods like the IC stripline and considerable power is required to obtain sufficient field strength to determine the susceptibility of ICs. We also showed that, as expected, adding tracks to the IC under test significantly increases the susceptibility. Since most real designs have tracks on the outer layers the immunity levels measured using stripline techniques are much higher than would be achieved in real equipment. It has also been shown that when using the frequency steps suggested in the standard some underlying and undersampled effects could produce rather strange measurement results. We had to use frequency steps 1000 times smaller than suggested in the standard to see the detail of these effects. The effects themselves seem to be related to the clock frequency of the A/D converter but the reasons for this are still beyond our understanding. We also note that digital ICs are commonly said to be susceptible to frequencies related to their clock frequency – here we found the opposite to be true.

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