Quantum-Well Design for Monolithic Optical Devices With Gain and Saturable Absorber Sections

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***Abstract*—We propose a new design of semiconductor quantum-well heterostructures, which can be used to improve the performance of monolithic mode-locked diode lasers and all-optical signal-processing devices with gain and saturable absorber sections. Numerical modeling shows that this design can increase the carrier sweep-out rate from the absorber section by several orders of magnitude, while retaining high carrier confinement on the ground level making for efficient signal amplification by the gain sections.**

***Index Terms*—Optical signal processing, optoelectronic devices, quantum wells (QWs), saturable absorbers (SAs).**

IN RECENT years, there has been considerable progress in the research and development of monolithic optoelectronic heterostructure devices such as mode-locked lasers (for an overview, see [1]) and all-optical signal processing devices [2]–[4]. The device implementation of such structures can drastically increase optical-network capacity by performing functions such as high bit rate pulse generation, all-optical clock recovery, and pulse regeneration.

A monolithic semiconductor device, potentially capable of performing all-optical signal processing, will be based on a laser-type heterostructure containing at least two electrically separated sections of the waveguide, arranged in tandem. One of the sections is forward-biased and performs amplification functions, and the other reverse-biased section works as a saturable absorber (SA) unit.

The most common designs of such devices implemented up to date use multiple quantum-well (QW) heterostructure, with small-to-moderate QW depth [5]. The limitation on the QW depth is imposed by the requirement of a short SA recovery time, ideally down to single picoseconds. In most applications, this time constant determines the maximum operational frequency of the device. As was established by previous experimental and theoretical work [6] and confirmed by our calculations [7], the main escape mechanism from an SA at room temperature has a thermal-activation nature. The SA recovery time increases exponentially with the depth of the QW.

However, it is well known that increasing the QW depth can decrease recombination carrier loss in the optical confinement layer (OCL). The value of the optical gain in amplification section would increase and its temperature sensitivity would decrease with the enhancement of the carrier localization [8]. Large QW-to-OCL escape times can decrease carrier leakage from the OCL. While heterostructures with increased carrier confinement, such as GaInAs–AlGaInAs and InGaAsN–GaAs, are being developed, the apparent fundamental short-escape-time limitation may pose an obstacle for the use of such materials for high-quality optical monolithic devices with SAs.

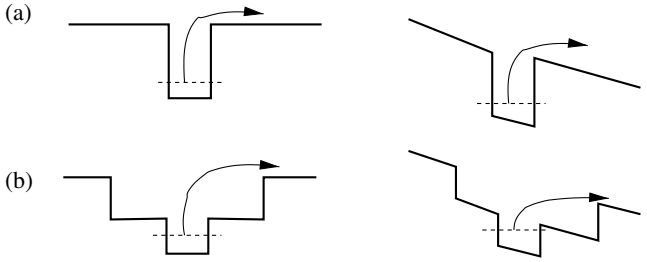

Fig. 1. Illustration of an idea for the design modification. (a) Unbiased and biased single-QW structure. (b) Unbiased and biased step-like structure.

We propose a new QW heterostructure design for a monolithic device with gain and SA sections on the same chip. It is intended to combine the high carrier localization of a deep QW with short carrier sweep-out times at the operational reverse bias. One of the possible implementations of such a structure is shown in Fig. 1(b). At zero bias, the electron on the ground level of the step-like structure depicted in Fig. 1(b) faces approximately the same barrier height as the electron in the deep QW [Fig. 1(a)]. When a significant electric field is applied, the barrier height for the step-like structure is much lower then for the conventional single-QW one. The same argument holds for holes. This should ensure high carrier localization for the gain section and short absorption recovery time for the SA section. The trapezoidal and triangular structures depicted in Fig. 2(c) and (d) are based on the same idea.

To test our proposal theoretically, we need an efficient method for calculation of the carrier escape time for an arbitrary QW profile and applied electric field. Most of the previously employed approaches are either too approximate [9], [10] or computationally difficult [11]. Here, we use the simple and computationally efficient yet quite rigorous theory of carrier escape from semiconductor heterostructures developed in our previous work [7]. Our method treats both tunneling and thermionic emission on the same footing. We use single-band effective-mass approximation, the electron levels are supposed to be in quasi-equilibrium, and only coherent tunneling processes are considered, i.e., the coherence length is supposed to be larger than the characteristic width of the structure. The gradient layers in the trapezoid and triangular structures are described by constant mean

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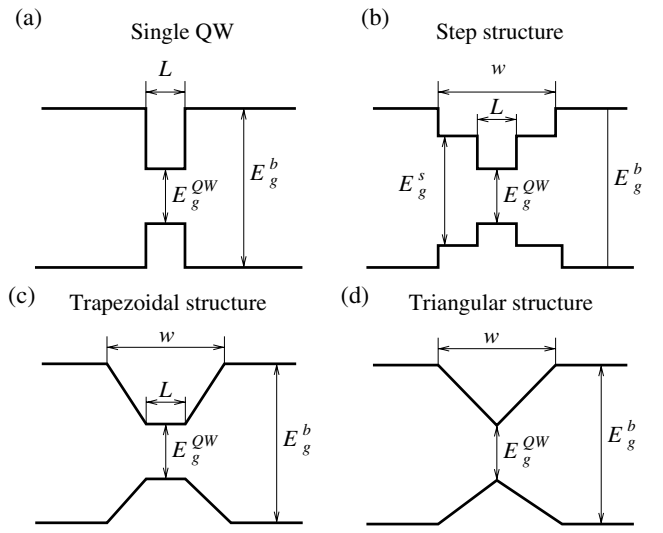

Fig. 2. Conductance and valence bands of four types of heterostructures under consideration.

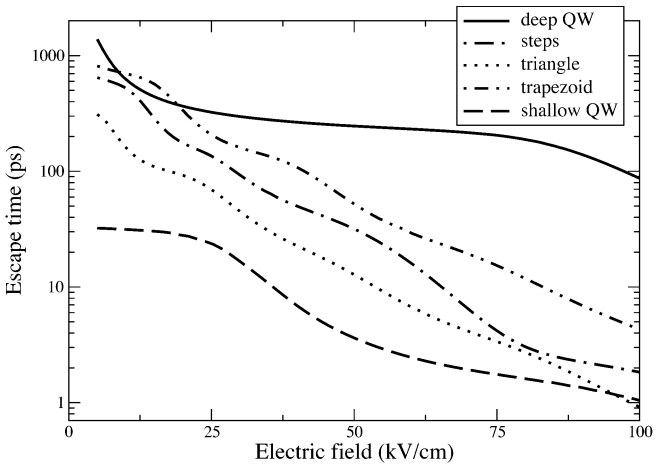

Fig. 3. Calculated electron escape time from different structures as a function of applied electric field. The width parameters L and w are equal to 10 and 30 nm, respectively. The deep QW has 0.3 and the shallow QW has 0.18 aluminum percentage in the barriers.

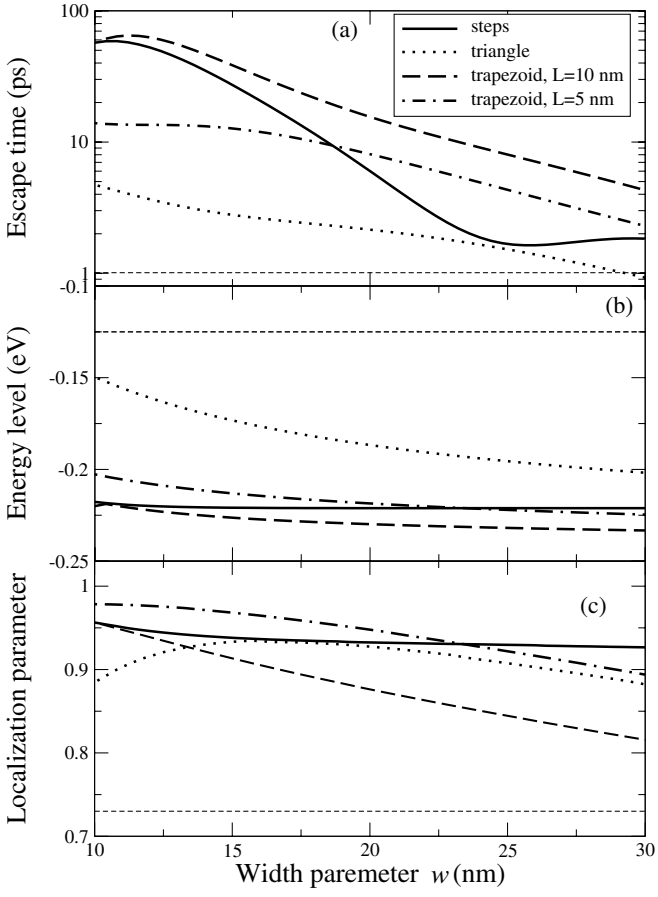

Fig. 4. (a) Electron escape time at $F = 100$ kV/cm, (b) electron ground level measured from the bottom of OCL conduction band, and (c) localization parameter as a function of the width w for different structures. The thin dashed lines show the values of the corresponding parameters for the shallow QW.

effective masses. No additional approximations are involved. Choosing appropriate boundary conditions, we derived the following expression for the electron escape-current density: $J_e = \int J_e(E)dE$, where

$$J_e(E) = \frac{e}{2\hbar\pi}\frac{|t(E)|^4 P(E)}{|1 - r_+ r_-(E)|^2}. \quad (1)$$

Here, $t(E)$ is the complex amplitude coefficient of electron transmission from inside the structure to infinity and r_+ (r_-) are the reflection coefficients for electrons propagating inside the structure to the right (left). These coefficients can be expressed exactly in terms of Airy functions. The function $P(E^b)$ coincides with the density of electrons on the quasi-bound level E^b; in quasi-equilibrium, it is calculated as $P(E) = m_e/(\beta\hbar^2\pi)\ln(1 + \exp(\beta(\mu_e - E)))$, where $\beta = (k_B T)^{-1}$, m_e is the electron effective mass, and μ_e is the electron quasi-Fermi level. The electron escape time is determined as the ratio of the electron density n_e to the escape current J_e: $\tau = (en_e)/J_e$. Further details of our method and its rigorous derivation will be presented elsewhere [7].

We consider $Al_xGa_{1-x}As$ material with the following parameters: bandgap energy $E_g = 1.424 + 1.247x$; electron effective mass $m_e = 0.067 + 0.083x$; the band offset ratio between GaAs and AlGaAs was taken as 67/33 [12].

In case of holes, one should devise a more elaborate theory in order to account for band mixing, nonparabolicity, and heavy-to-light (light-to-heavy) hole transformation in tunneling processes. This will be the subject of our future work. In the meantime, we assessed the hole escape using different in-plane and transverse masses for different energy levels [7] and found that in the AlGaAs system, the hole escape time is generally several times lower than the electron escape time. This is mainly due to the fact that in this material band offsets for holes are much lower than for electrons, whereas the difference between the values of electron and light-holes effective masses is not large. Therefore, in what follows, we consider only electron escape time to assess the SA recovery time.

Note, that the electric field in Figs. 3 and 4 is the local value at the QWs. The effects of carrier-induced field screening will reduce the local field for a given bias at high carrier densities.

We have calculated the electron escape time (Fig. 3) for different types of structures presented in Fig. 2(a)–(d). In all the examples, E_g^{QW} is equal to the band-gap width of GaAs, the

barrier (E_g^b), and the step (E_g^s) are fabricated of $Al_xGa_{1-x}As$ with $x = 0.3$ and $x = 0.18$, correspondingly.

Confirming our qualitative considerations, when the applied electric field is high (about 100 kV/cm), all three proposed structures give the escape time one to two orders of magnitude lower then that of the deep single-QW SA, yielding the SA recovery time of units of picoseconds, i.e., close or even lower than that of conventional shallow QW design. Trapezoidal and step-like structures have the escape time at low fields of the same order as that for the deep single-QW structure, in accordance with the intuitive picture (see Fig. 1). This property can help reduce carrier leakage and recombination losses in the OCL, compared to the shallow QW structure, where the electron escape at low applied fields is fast. The triangular structure, which features the fastest escape at large applied fields, suffers however, from an undesirable decrease of the escape time at low fields. This is caused by the fact that the triangular shape of the potential well pushes the energy levels upwards, "squeezing" them out of the QW.

Obviously, if one takes $w = L$, the trapezoidal and step-like structures become equivalent to a single-QW structure. On the other hand, as can be seen from Fig. 1(b) and Fig. 3, increasing w will drastically decrease the escape time at large applied fields. However, w cannot be taken too large. Indeed, if in the step-like structure w is comparable to the OCL width, it effectively becomes a single-QW structure with a shallow QW as the active medium, whereas triangular and trapezoidal structures lose their two-dimensional properties, becoming effectively three-dimensional (3-D) as w increases. To account for this, it is useful to introduce the confinement parameter γ_e as the ratio of the density of the carriers on the ground size-quantized level to the total carrier density

$$\gamma_e = \frac{P\left(E_0^b\right)}{\sum_{i=0}^{n} P\left(E_i^b\right) + n^{3-D}d}. \tag{2}$$

Here n^{3-D} is the 3-D density of carriers in the OCL and d is the width of this layer (d is taken to be 0.35 μm). This parameter is dependent on the total carrier density in the system; here, the quasi-Fermi level was taken to be 1 kT below the ground electron level.

In Fig. 4, we plot the dependence of the parameters of the structures on the width w. As can be seen from Fig. 4(a), for all structures, the electron escape time τ decreases rapidly as the width w increases. In the case of the step-like structure, τ drops down to values approximately equal to the time of electron escape from a shallow, GaAs–$Al_{0.18}Ga_{0.82}As$, QW (approximately 1 ps), and does not decrease any more. On the other hand, trapezoidal and triangle structures show a monotonic decrease in the recovery time with w.

The ground electron level shows better localization than that of the shallow QW in all the structures under consideration. For the step-like structure, the energy position is approximately equal to, and for the trapezoid with $L = 10$ nm even lower than, that of the deep QW. The shorter trapezoid base ($L = 5$ nm or 0 in case of triangular structure) leads to greater influence of the "squeezing" effect.

At large w, localization parameters of all the structures show a decreasing trend, which is due to the increase of the number of levels in the QWs. One can see that the localization parameters of the proposed structures are substantially larger than that of the shallow QW. Comparing the localization parameter of the trapezoid structure with different bases, one can deduce that there is an interplay between the enhancement of the energy distance between quantized levels and the decrease of the ground-level localization as the base is shortened. Indeed, the trapezoid with $L = 5$ nm has a larger localization parameter than that of $L = 10$ nm, whereas, the triangular structure ($L = 0$) has a decreased value of γ at small w, which is due to the ground level "squeezing."

In conclusion, we have proposed a novel design of semiconductor quantum-well heterostructures to be used in monolithic optoelectronic devices with gain and SA sections. Numerical modeling has shown that the values of electron escape time on the order of single picoseconds under realistic reverse bias can be achieved in such structures, while the ground level in the gain section can be made more than 100 meV deeper than that of conventional structures, showing much better carrier localization.

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