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# PMBS 2016: 7th International Workshop on Performance Modeling, Benchmarking and Simulation of High Performance Computing Systems


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# 7th International Workshop on Performance Modeling, Benchmarking and Simulation of High Performance Computing Systems (PMBS 2016)

This volume contains the 11 full papers presented at the 7th International Workshop on Performance Modeling, Benchmarking and Simulation of High Performance Computing Systems (PMBS 2016), held as part of the 28th ACM/IEEE International Conference for High Performance Computing, Networking, Storage and Analysis (SC 2016) at the Salt Palace Convention Centre in Salt Lake City, Utah on 13-18 November 2016.

The SC conference series is the premier international forum for high-performance computing, networking, storage and analysis. The conference is unique in that it hosts a wide range of international participants from academia, national laboratories and industry, and featured over 350 exhibitors in the industry's largest HPC technology fair.

This year's conference was themed *HPC matters*, with a focus on the importance of HPC in a range of scientific endeavours. Today, HPC is being used in a variety of fields including epidemiology, engineering, nuclear research and meteorology. HPC is enabling us to predict the spread of diseases, optimize and verify the designs of car and aeroplane engines, simulate the conditions present at the big bang and provide ever more accurate predictions of future weather conditions. HPC has an influence on every aspect of modern life.

SC offers a vibrant technical program, which includes technical papers, tutorials in advanced areas, Birds of a Feather sessions (BoFs), panel debates, a doctoral showcase and a number of technical workshops in specialist areas (of which PMBS is one).

The focus of the PMBS 2016 workshop was comparing high-performance computing systems through performance modeling, benchmarking or the use of tools such as simulators. We were particularly interested in receiving research papers which reported the ability to measure and make trade-offs in hardware/software co-design to improve sustained application performance. We were also keen to capture the assessment of future systems, for example through work that ensured continued application scalability through peta- and exa-scale systems.

The aim of the PMBS 2016 workshop was to bring together researchers from industry, national laboratories and academia, who were concerned with the qualitative and quantitative evaluation and modeling of high-performance computing systems. Authors were invited to submit novel research in all areas of performance modeling, benchmarking and simulation, and we welcomed research that combined novel theory and practice. We also expressed an interest in submissions that included analysis of power consumption and reliability, and were receptive to performance modeling research that made use of analytical methods as well as those based on tracing tools and simulators.

Technical submissions were encouraged in areas including: performance modeling and analysis of applications and high-performance computing systems; novel techniques and tools for performance evaluation and prediction; advanced simulation techniques and tools; micro-benchmarking, application benchmarking and tracing; performance-driven code optimisation and scalability analysis; verification and validation of performance models; benchmarking and performance analysis of novel hardware; performance concerns in software/hardware co-design; tuning and auto-tuning of HPC applications and algorithms; benchmark suites and proxy apps; performance visualization; real-world case studies; studies of novel hardware such as Intel Xeon Phi coprocessor technology, NVIDIA Kepler GPUs and AMD Fusion APU.

## PMBS 2016

We received an excellent number of submissions for this year's workshop. As a result of this we were able to be very selective in those papers that were chosen; 11 full papers were accepted from a total of 49 submissions (22%). The resulting papers represent worldwide programs of research committed to understanding application and architecture performance to enable peta-scale computational science.

Contributors to the workshop included the University of Alabama at Birmingham, the University of Basel, the University of California at Davis, the University of Copenhagen, Cray Inc., Google, the IBM Thomas J. Watson Research Center, Intel Corporation, Lawrence Berkeley National Laboratory, Lawrence Livermore National Laboratory, Oak Ridge National Laboratory, Rice University, University of Stuttgart and ETH Zürich.

Marjanović et al. use multiple different datasets with HPCG and HPGMG to demonstrate the effect of problem size on building machine ranking lists. On the theme of benchmarking, Chen et al. evaluate multiple supercomputing interconnects and show how moving to more complex interconnects (such as the Dragonfly interconnect) may be more or less cost-effective for a variety of workloads.

Gahvari et al. discuss the use of an alternative approach to solving time-dependent problems by parallelising over time, in addition to space. They propose a performance model that solves the question of how much parallelism to allocate to the time domain versus the space domain. Similarly, Yeom et al. propose a performance model enabling users to identify the fastest preconditioner and solver for a given input matrix ahead of execution.

One emerging feature of modern HPC systems is the use of accelerator architectures such as GPUs and the Intel Xeon Phi. On this theme, Barnes et al. present an analysis of the NERSC workload on the new Intel Xeon Phi Knights Landing architecture. Their current analysis shows improved performance for memory bandwidth bound applications and more modest gains for other applications. Martineau et al. use an NVIDIA Kepler GPU to evaluate the performance of the Clang compiler's OpenMP 4.5 implementation. Our final accelerator evaluation paper, by Yount et al., demonstrates how to effectively use the high bandwidth memory (HBM) present on the new Xeon Phi architecture. Their implementation of a 3D stencil application shows a significant speed up on HBM when compared to standard DDR memory.

Yuhan Peng and colleagues also make significant use of GPUs in their work, proposing a performance model that can be used to evaluate a variety of data layouts and their effects on performance. Ross et al. build on their previous work on the ROSS simulator to provide visual data analytics for large-scale parallel discrete-event simulations.

In our penultimate paper, Pearce et al. develop the CoMD proxy application to investigate the use of work migration to improve load imbalance. The final paper presented at PMBS this year, by Guerrero et al., details the use of their PROVA! tool to evaluate a stencil benchmark. They also focus their attention on the issue of reproducibility — one of the major concerns of current HPC research.

## Acknowledgements

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Stephen A. Jarvis
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(on behalf of the PMBS 2016 Program Committee)

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