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A Cost-Effective Technique for Concurrent IQ stream Capture for Prototyping Phased Arrays

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Abstract

This paper introduces a new and affordable method of realising 10 IQ Software Defined receivers, and how to synchronise them. We first discuss the need for mulitple IQ and the availiable techniques. We then introduce the RTL-SDR and Matlab as a very low cost prototype implementation of 10 IQ streams. This leads to the design and manufacture of a PCB to distribute a single clock to multiple RTL-SDRs. The required modifications to the RTL-SDRs to receive the distributed clock and other modifications to improve the overall performance are presented. We then describe how to attain raw IQ data and synchronise the receivers. Finally, we prove all 10 can maintain a phase lock over a frame of 7 seconds.

1 Introduction

With over ten thousand MIMO related published papers in the last three years at the IEEE alone, only a small number of researchers have a chance to apply their early stage concepts and test it in the real world. Further applications, such as the Microsoft's recent Indoor Localisation competition [1], conclude that indoor localisation is still a hot topic and further research is required. The Angle of Arrival (AoA) is one solution requiring synchronised receivers to measure the phase difference between them and subsequently apply a diverse range of Digital Signal Processing. Systems such as ArrayTrack [2] utilise spatial diversity and achieve cm level accuracy.

Conventional research platforms for concurrent IQ stream data capture can be prohibitively expensive for early-stage proof of concept research and development. A single two channel Software Defined Radio (SDR) can cost circa £1300 [3] while a four channel SDR transceiver adapter module for the NI-PXI platform alone is circa £2770 [4].

The RTL-SDR is a popular, low-cost USB TV Tuner [5] with a cost less than £17. It has found application in recent years by educators [6] and in many published applications e.g. [7-8]. Matlab now supports multiple concurrent instantiations of the RTL-SDR, which raises the attraction of its application to the capture of phase-aligned RF data. This paper describes the approach we have taken to modify R820T2 RTL-SDRs (priced less than £7), to achieve phase lock between 10 modules and how this can then be used to implement low-cost phase aligned data capture. Matlab officially supports designing and prototype SDR systems using Matlab and Simulink [9]. From our understanding Matlab supports the existence of multiple RTL-SDR with no upper limitation.

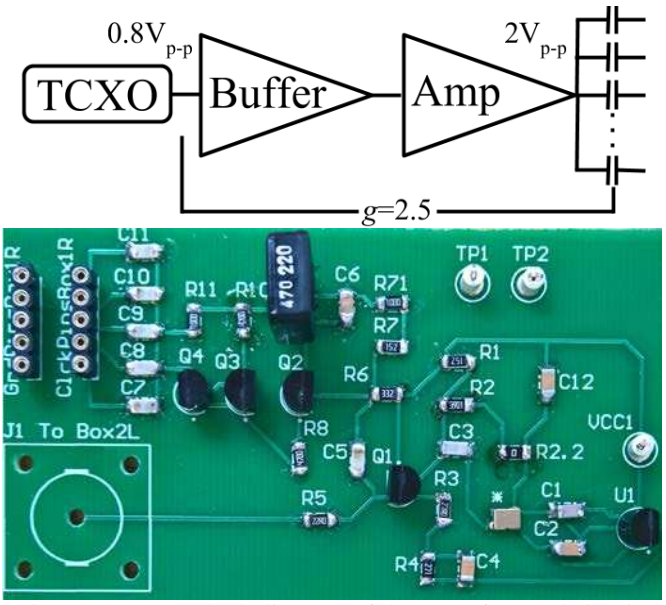

Figure 1: (Top) Block diagram of the manufactured circuit. (Bottom) Manufactured and assembled 28.8MHz reference distribution amplifier.

The paper is organised as follows: Section 2 presents the phase lock reference and modifications to improve the performance of the RTL-SDRs. Section 3 is dedicated to the time alignment of the ten RTL-SDRs, in Section 4 we discuss the result and in Section 5 we conclude and suggest some next steps.

2 Phase lock reference and improvements on the RTL-SDRs

This section is split into two subsections. At Subsection 2.1 we provide the necessary information to manufacture the required hardware to achieve phase lock over 10 RTL-SDRs and Subsection 2.2 is dedicated to hardware improvements and optimizations that can be applied on the RTL-SDRs.

2.1 Common oscillator source

To synchronise sampling and carrier oscilator phase of multiple RTL-SDRS, a common clock source is necessary. To reduce temperature sensitivity and maintain a low cost, a

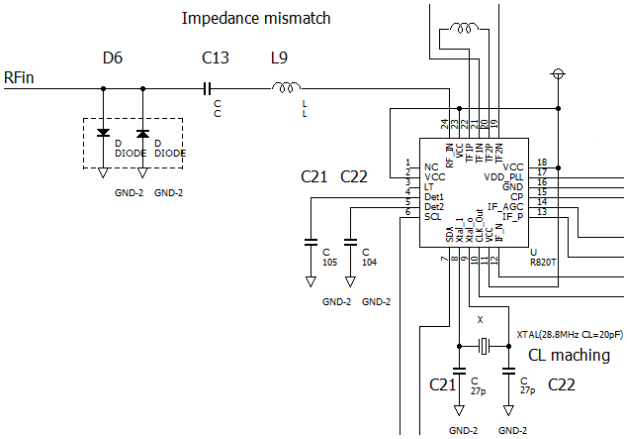

Figure 2: Part of the RTL-SDR full schematic [11] for modifications reference.

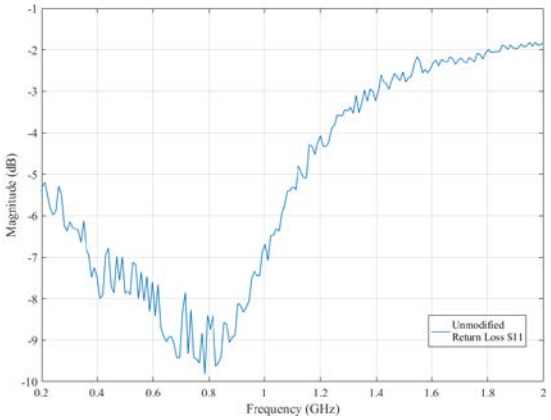

Figure 3: Return loss of an unmodified R820T2 RTL-SDR with TV connector.

Temperature Compensated Crystal Oscillators (TCXO) is favoured. For this application, the TCXO output at 28.8 MHz [10] was first buffered and amplified as seen in Figure 1 (Top). With a TCXO output being at 0.8 $V_{p\text{-}p}$ and the oscillator voltage of an unmodified RTL-SDR measured at 2 $V_{p\text{-}p}$ the required gain is g=2.5. The R820T2 chip self-biases its oscillator input pin, so only AC coupling is required. Figure 1 (Bottom) shows part of the PCB manufactured and assembled for our purposes. We split the circuit into two boards, where each one services 5 RTL-SDR. This configuration offers the versatility that is necessary for a 10-antenna configuration, minimising the cable lengths

2. 2 Modifications to the RTL-SDRs

For the sake of space, we cannot provide the full schematic of an RTL-SDR [11]; for notation purpose in Figure 2 we show some parts that are referenced for modifications. Every RTL-SDR requires a simple hardware modification to connect the common oscillator source. After the removal of the through-hole on-board crystal oscillator (XTAL) and the SMT capacitors (C21, C22) we attach a pin and feed the signal from the TCXO distribution amplifier PCB to pin 8 of the R820T2 chip. Furthermore, all RTL-SDR require a common ground. We make sure that the length of the cables connecting the ground and clock from PCB to each RTL-SDR are at minimum to decrease losses and noise pick up.

The commercial RTL-SDR is manufactured to service a large bandwidth; Figure 3 shows the return loss S11 of an unmodified RTL-SDR with a TV connector. We can see that S11 is between -8 dB and -10 dB from 600 to 900 MHz which makes the RTL-SDR efficient at those frequencies. To optimise the RTL-SDR, we can perform further modifications such as replacing the TV connector with an SMA and tuning the on-board matching network. The on-board matching network is a series LC circuit (C13, L9) after the RF connector (RFin) as seen in Figure 2. Depending on the frequency of the application we can design and apply the appropriate matching network using the available pads (C13, L9) on board or directly on the SMA connector or adapt the PCB.

3 Sample Time Alignment

Due to computer operating system latency and scheduling, the actual start of sampling at each RTL-SDR is not deterministic. This uncertainty must be removed by measuring the time delay experienced by each RTL-SDR using a known standard. To the best of our knowledge Matlab cannot operate more than one RTL-SDR without a Parallel Pool license or Simulink. Choosing any of those two solutions will increase the overall CPU load which will further increase the systems' latency. To overcome this, we create and edit a batch file through Matlab running the command *rtl_sdr* in Windows' command line with the appropriate parameters. This command is available for Windows through Matlab's Communications System Toolbox Support Package for RTL-SDR Radio Add-On [9] and it is only required to be added to the PATH environment variable. The number of connected RTL-SDRs and their buffer size plays an important role in reliability of data transfer.

We implemented an anchor node concept that was in a defined position and used as a reference phase for all RTL-SDRs. The anchor node can also be a leaky-feed directly into the RTL-SDRs, periodically enabled to synchronise each frame. Using the anchor that transmits a known signal, we cross-correlate each received signal from all the RTL-SDRs, find the RTL-SDR with the highest delay and synchronise the remaining RTL-SDRs. We can then subtract the known signal sequence and have a phase synchronised IQ data from the 10 receivers for the remainder of the frame. This process must be repeated for each received frame, as the delay is not maintained between frames.

4 Results and Discussion

We have measured the phase alignment of the IQ framed data from 10 RTL-SDRs aligned to a reference anchor. We used an SPIRIT1 low rate transceiver [12] as an anchor node transmitting an OOK signal at a carrier frequency of 869.05 MHz, with a data rate of 500 bps, an output power of -70 dBm. For simplicity, we only present the In-phase components in time in Figure 4 (a) rather than both In-phase and Quadrature. The presented frame is a conductive

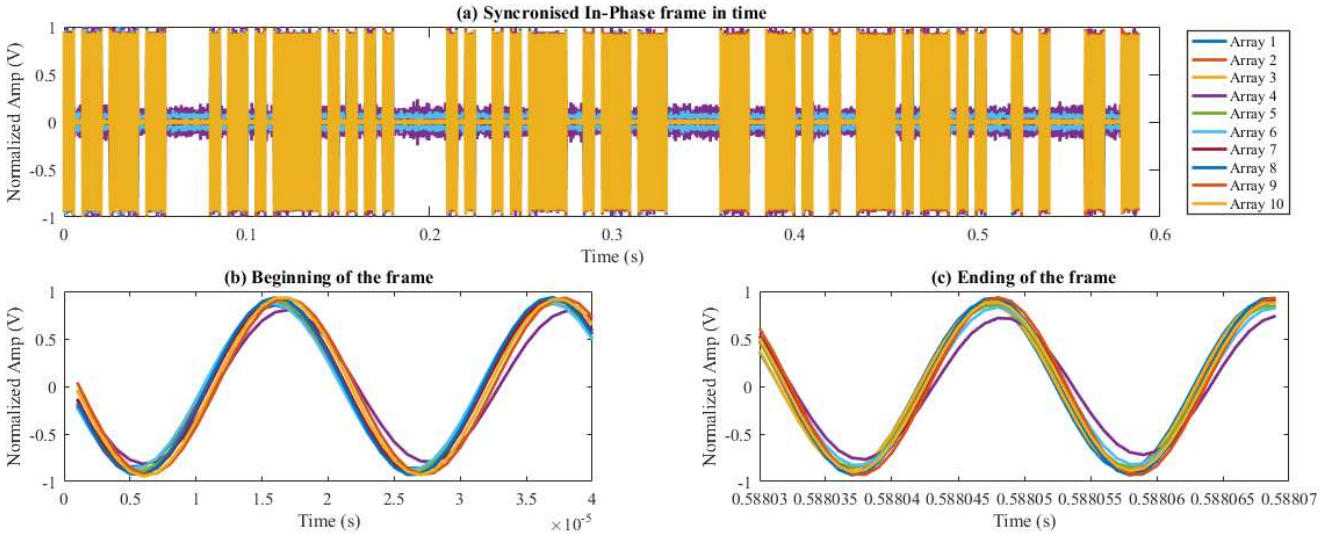

Figure 4: (a) Synchronized received In-phase frame that shows the phase alignment in the (b) beginning and (c) ending of the frame.

measurement of the OOK modulation signal at an Intermediate Frequency of 50 KHz, 1 Meg. sample rate, and buffer size of 2800 samples. The original captured frame was consisted of 10 Meg. samples but reduced to 6 Meg. samples due to the time samples required for synchronisation. A coarse time alignment can be observed from the overall frame. Figure 4 (b) is the beginning of the frame from 0 s to 40 µs that shows all 10 In-phase streams synchronised while Figure 4 (c) is the ending of the same frame from 588.03 ms to 588.07 ms. This proves all 10 In-phase streams keep their phase alignment. The same results can also be seen for the Quadrature components.

During tests, we discovered that each RTL-SDR stream had a different amplitude. This difference can be attributed to the sensitivity variability between the RTL-SDRs. The greatest difference seen is -8 dB, well within hardware tolerances and easily calibrated out, as we have done on the above figures.

5 Conclusions and future applications

In this paper, we showed that the RTL-SDR is a compelling platform for low-cost early stage research concepts that require phase aligned IQ data frames. We have given a block diagram and shown the manufactured PCB circuit required to perform phase synchronisation for multiple RTL-SDRs, presented the return loss of a commercial unmodified RTL-SDR and proposed modifications. Finally, we proved that ten RTL-SDRs maintain phase lock throughout the frame of 0.6 seconds, using our technique.

The proposed system can be used as a multiple input receiver allowing us to perform measurements and apply any DSP required within Matlab environment. A future application could be a 10 antenna localization system for applying different techniques as a testbed to create new algorithms.

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