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https://doi.org/10.1109/LED.2017.2747898

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An E-mode p-channel GaN MOSHFET for a CMOS compatible PMIC

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Abstract—The operation principle of a low power E-mode p-channel GaN MOSHFET is explained via TCAD simulations. The challenges of achieving negative threshold voltage with the scaling of gate length are addressed by adjusting the mole fraction of an AlGaN cap layer beneath the gate. An inverter consisting of the proposed p-channel GaN MOSHFET with a gate length of 0.25 μm shows promise of a CMOS compatible Power Management IC in the MHz range.

Index Terms—2DHG, Enhancement mode, Gallium Nitride, p-channel MOSHFET, superjunction, inverter, switching speed.

I. INTRODUCTION

Among the various techniques for overcoming the trade-off between the on-resistance and breakdown voltage in a high power device in GaN, polarization superjunction (PSJ) technology [1], [2] is an attractive solution which can be considered as the equivalent of CoolMOS in silicon [3]. The presence of a polarization induced 2DHG above the 2DEG across the barrier layer forms a superjunction which helps prevent current collapse by suppressing the non-linear current density of the electric field around the drain-side gate edge, [1], [2] thus improving the reliability.

The next challenge for GaN power devices is integration of the gate driver and power device, to reduce the parasitic loop inductance and facilitate high frequency switching in converters [4], [5]. Additionally, complementary logic with normally-off (E-mode) operation is preferred to reduce static power consumption, simplify circuitry and for fail-safe operation [6]. Therefore, a p-channel E-mode GaN MOSHFET is desirable.

The inherent use of the 2DHG in a PSJ heterostructure (GaN/AlGaN/GaN or GaN/AlInGaN/GaN) makes it a suitable platform for such integration. The operation of both p-channel and n-channel devices has been demonstrated on this platform [4], [7]. Achieving E-mode operation in GaN is challenging because the polarization induced 2DEG or 2DHG first needs to be depleted at zero gate voltage. In n-channel GaN HFETs or MOSHFETs, various techniques to implement E-mode behaviour are recessed gate [8]–[10], or ion implantation [11]–[13]; both methods can be employed on a PSJ platform. On the other hand, less attention has been paid to p-channel devices due to the low mobility of holes in GaN (~16 cm²/v·s at room temperature [14]), which leads to poor on-current and switching speed. E-mode operation of p-channel HFETs has been attempted via recessed gate [5], [15], [16], an Al₂O₃ separated gate on a GaN/AlN heterostructure [17], or reducing the polarization charge in GaN/AlN/GaN heterostructures by adjusting the Al or In mole fraction [18]. However, except for the recessed gate approach, the others have similar challenges associated with optimisation of the substrate layers for all other devices on the platform. These choices can lead to deterioration of the performance and reliability of the power devices by reduction in density of the 2DEG/2DHG respectively. Moreover, even with a recessed gate, we have earlier demonstrated a trade-off between the threshold voltage $V_{th}$ and the on-current $I_{on}$ in the conventional p-channel MOSHFET that can be addressed by a thin AlGaN cap layer beneath the gate, to achieve better control [19]. In this work, the dependence of the electrical characteristics of a p-channel GaN MOSHFET on gate length is investigated on a platform that is fully compatible with a power device in PSJ technology. The substrate parameters are closely aligned to those reported in [5], [15]. Subsequently the switching speed of the inverter is evaluated.

II. METHODOLOGY AND SETTINGS

Fig. 1 highlights a schematic of an integration platform consisting of low power CMOS and High Power PSJ MOSHFET. The 2DEG is connected to the ground. A combination of the 2DHG, AlGaN barrier, and 2DEG forms a diode that remains reverse biased.

The work was partially funded by ENIAC-JU project E2SG.
performed in Silvaco TCAD [22] using our model for the hole transport in p-channel GaN devices, calibrated against the experimental results of [15]. Accordingly, the maximum hole mobility is limited to 16 cm²/Vs [14] in a field dependent mobility model [23]. Additionally, a contact resistance ρc of 10⁻⁴ Ωcm² is used for source and drain contacts to p-GaN, which is an average contact resistance reported for p-GaN [24]. Charge and trap densities of 2.8 × 10¹² cm⁻² and 2.5 × 10¹² cm⁻² at oxide/GaN interface are found sufficient to match the experimental I_DS – V_DS characteristics reported in [15].

III. RESULTS AND DISCUSSIONS

E-mode operation in a conventional heterostucture without an AlGaN cap, may be examined by comparing the band diagrams at two different thicknesses of the oxide and channel layers (t_ox & t_D) in Fig. 2(a). Thinner oxide and GaN channel are required so that, sharp band bending in these layers can prevent the valence band at the GaN/AlGaN heterointerface from crossing the Fermi level, thus giving E-mode behaviour. The transfer characteristics of devices in Fig. 2(c) reveal that without the presence of the AlGaN cap, the thicknesses of the oxide and GaN channel layers (t_ox & t_D) need to be reduced to ~5 nm to increase the [V_th] to |−1.4| V. Such low values introduce considerable constraints on the manufacturability of the conventional structure. Owing to the trade-off between [V_th] and I_ON, the maximum drain current [I_ON], for the structure with AlGaN cap, at a higher [V_th] of |−2| V remains smaller (25 mA/mm) than that of the structure without an AlGaN cap at a smaller [V_th] of |−1.4| V (62 mA/mm). The trap charge at the interface of the oxide and AlGaN cap could vary due to processing or during device switching. Fig. 2(d) compares the transfer characteristics with the change in the net trap density at the interface of the oxide/AlGaN cap σ_ox, showing that a large variation in σ_ox (> 7 × 10¹¹ cm⁻²) can significantly affect the V_th and on-off current ratio of the device.

As shown in Fig. 1, a combination of the 2DHG, AlGaN barrier, and 2DEG acts as a p-n diode, where the AlGaN barrier of 47 nm acts as a depletion region between the 2DEG and 2DHG. With negative voltage on the drain and gate, this diode remains reverse biased, and leakage current through the 2DEG in this condition has been experimentally shown to be |−10 nA/mm| through the AlGaN barrier [25]. This agrees with negligible values in the simulations.

The behaviour of the threshold voltage with the Al mole fraction x_cap, in Fig. 3(a), depicts a rise in [V_th] with x_cap. As higher x_cap, the band bending in the GaN channel becomes more pronounced due to an increase in polarisation σ_cap, leading to a lowering of the valence band at the GaN channel/AlGaN barrier interface. A [V_th] of |−3.0| V is achievable for an x_cap of 23%.

In contrast, inclusion of an AlGaN cap introduces a positive polarization charge at the heterointerface between the AlGaN cap and the GaN channel, σ_cap, which can be controlled by changing the Al mole fraction in the cap layer x_cap. A comparison of the band diagrams with and without the AlGaN cap in Fig. 2(b), illustrates that a presence of the polarisation charge σ_cap increases band bending in the GaN channel, leading to elimination of the hole quantum well at the GaN/AlGaN interface. This consequently leads to E-mode operation for thicker layers of the channel and oxide in comparison to that in the conventional structure. It can also be noted in Fig. 2(b) that the introduction of σ_cap alters the direction of the electric field in the oxide. This is of crucial benefit that reverses the behaviour of [V_th] with respect to t_ox as opposed to that in the conventional device [19].

In comparison to silicon, the V_th of the current heterostucture is not just dependent upon the vertical thicknesses but also severely the gate length L_g. It is seen in Fig. 3(b) that with reduction of L_g, a higher x_cap is required to maintain the [V_th] at |−2| V. To understand this behaviour, the
gate and drain capacitances for the p-channel GaN MOSHFET, are presented in Figs. 3(c) & 3(d) for two different gate lengths (0.25 μm and 8 μm). The dependency between \( V_{th} \) and \( L_G \) arises from the fact that a 2DHG forms at the bottom interface of the GaN channel which is farther from the gate rather than at the top interface. Hence, even though holes in the vicinity of the top interface. Hence, even though holes in the vicinity of the gate thereby minimizing the leakage current. Hence, the gate length of

\[ t_{rise} = (t_{rise} + t_{fall})^{-1} \approx (2 \cdot t_{rise})^{-1} \]  

yields a value of \( \sim 625 \text{ MHz} \) for a \( C_L \) corresponding to a fanout of 5.

Compared to a \( t_{rise} \) of 670 ns, reported by R. Chu et al. [5] for their fabricated p-channel device, a significantly smaller \( t_{rise} \) is the result of much smaller on-resistance \( (R_{on}) \) and load capacitor of 143 Ω·mm and 33 P F/mm compared to their values of 1314 Ω·mm and \( C_L \) estimated \( t_{rise}/2.2R_{on} = 231 \text{ pF/mm} \), respectively from their work. Our smaller on-resistance is the result of higher on-current facilitated by lower access resistances and depletion beneath the channel, facilitated by the AlGaN cap. If their value of \( C_L \) of 231 pF/mm were employed, the corresponding rise time is predicted to be 56 ns, an improvement of at least a factor of 10 in switching speed.

### IV. Conclusion

A low voltage p-channel E-mode GaN MOSHFET for integration alongside a high power device on a common GaN/AlGaN/GaN platform is investigated. The E-mode operation is realised using a thin AlGaN cap layer between the GaN channel and gate dielectric that suppresses the penetration of holes beneath the channel. The technique not only improves the on-current but also suppresses the leakage current, leading to orders of magnitude improvement in on-off ratio at short gate lengths. The simulated inverter offers promise of CMOS integrated gate drivers for MHz switching of power conversion circuits in GaN.
REFERENCES


