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# A nanoionics based three terminal synaptic device using Zinc Oxide

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KEYWORDS : Zinc Oxide, synaptic thin film transistors, Tantalum oxide, Oxygen vacancies,  
Memory TFTs

ABSTRACT: Artificial synaptic Thin Film Transistors (TFTs) capable of simultaneously manifesting signal transmission and self-learning are demonstrated using transparent zinc oxide (ZnO) in combination with high  $\kappa$  tantalum oxide as gate insulator. The devices exhibit pronounced memory retention with a memory window in excess of 4V realized using an operating voltage less than 6V. Gate polarity induced motion of oxygen vacancies in the gate insulator is proposed to play a vital role in emulating synaptic behavior, directly measured as the transmission of a signal between the source and drain (S/D) terminals, but with the added benefit of independent control of synaptic weight. Unlike in two terminal memristor/resistive switching devices, multistate memory levels are demonstrated using the gate terminal without hampering the signal transmission across the S/D electrodes. Synaptic functions in the devices can be emulated using a

low programming voltage of 200 mV, an order of magnitude smaller than in conventional resistive random access memory and other field effect transistor based synaptic technologies. Robust synaptic properties demonstrated using fully transparent, ecofriendly inorganic materials chosen here show greater promise in realising scalable synaptic devices compared to organic synaptic and other liquid electrolyte gated device technologies. Most importantly, the strong coupling between the in-plane gate and semiconductor channel through ionic charge in the gate insulator shown by these devices, can lead to an artificial neural network with multiple pre-synaptic terminals for complex synaptic learning processes. This provides opportunities to alleviate the extreme requirements of component and interconnect density in realizing brain-like systems.

## 1. INTRODUCTION

The rapid development in mimicking memory or learning behaviour of biological systems in nanoscale ionic/electronic devices has spurred a great deal of interest in the scientific community in realising neuromorphic systems.<sup>1</sup> Despite these worldwide efforts, neuromorphic systems with similar levels of robustness in terms of energy efficiency, self-learning and scalability in emulating complex biological activities are yet to be realised.<sup>2</sup> At a cellular level, the nervous system is composed of neurons that are interconnected by synapses. A synapse is a specialized junction between two nerve cells, via which the signal from one neuron is transmitted to another.<sup>3</sup> The most significant property of a synapse is its plasticity, which is the ability to strengthen or weaken over time with respect to activity, known as synaptic potentiation and depression respectively.<sup>4</sup> Spike-Timing-Dependent Plasticity (STDP) (measured as the growth/decay of the excitatory post synaptic response based on the relative timing between pre and post spikes) and short-term

memory (STM) to long-term memory (LTM) transitions are considered as the two predominant synaptic learning rules.<sup>5,6</sup>

The emulation of an energy efficient neural behaviour at a single device level is a challenge that may well be considered daunting. In the quest for realising synaptic functions, software based neuromorphic approaches were first developed to create a mathematical model.<sup>7,8</sup> However, the energy efficiency of these approaches is limited due to the considerably higher power consumption of computing systems in emulating the complexity of a biological brain with  $\sim 10^{13}$  synapses.<sup>9</sup> The system and energy inefficiency of the traditional architectures are mainly rooted in their core concept known as the von Neumann architecture, where physically separated memory, processing and logic units are interconnected by bus paths. This architecture results in a bottleneck that requires continuous storage and retrieval of information from different parts of the system, making it one of the least energy efficient approaches. Hardware based approaches using Silicon neurons (SiNs) are found to be more energy efficient than software based approaches<sup>9</sup> and offer a real time large scale emulation of neurosynaptic behaviour. Recent development in hybrid complementary metal oxide- semiconductors (CMOS)/ two terminal memristor based neuromorphic systems, utilise a CMOS subsystem to address each memristor on the cross bar. This architecture presents opportunities to connect CMOS implemented spiking neurons with memristors that function like a biological synapse, where metal interconnects play the role of axons and dendrites.<sup>10-12</sup> However, the major challenge in realising large scale neuromorphic systems using this approach is the requirement of additional driving /pulse shaping circuitry to implement STDP behaviour in memristors. Moreover, the primitive circuit that captures the operation of a biological neuron in CMOS employs a capacitor that represents the neuron's membrane capacitance ( $C_{\text{mem}}$ ).<sup>13</sup> It requires integration of the input current and when the capacitor potential crosses the spiking

threshold, a pulse  $V_{out}$  is generated that resets the membrane potential  $V_{mem}$ . A simplistic implementation of an integrate and fire (I&F) neuron using SiN requires at least 6 components (CMOS transistors and capacitors)<sup>13</sup>, presenting a significant challenge for CMOS based approaches to achieve brain like systems with  $10^{11}$  neurons and interconnect (synapse) density between  $\sim 10^{11} - 10^{15}$  that is greater than any other manmade system.<sup>14</sup>

Neuromorphic systems require devices that respond in relation to their past history. This implies that these devices should have a multistate behaviour that responds at different levels to the same repetitive input stimuli depending on history. Non-volatility is another pivotal property requiring a capability of storing the memory/conductance state without any refresh or energy dissipation. Needless to say that they should have low energy dissipation and materials chosen should be compatible with mainstream technology. To realise physical devices with a synaptic function with low energy consumption and small foot print, two-terminal based resistive switches<sup>15,16</sup>, phase change memories<sup>17,18</sup>, conductive bridge devices<sup>19,20</sup>, ferroelectric thin films<sup>21,22</sup> and three-terminal field-effect transistors<sup>23-26</sup> have been proposed. Two terminal synaptic devices functioning as connecting elements between the pre and post neurons, have the limitation that signal transmission and learning functions cannot be carried out simultaneously. The learning function in two terminal devices are carried out by feeding the signal from the post neuron to the synaptic device terminal to modulate the synaptic weight while synaptic transmission is inhibited.<sup>17,18,25,28</sup> Moreover, synaptic weight modulation is mainly by engineering the pulse width and height by overlapping pulses, rather than frequency and relative timing of the spikes that is utilised in biological systems. However, three terminal synaptic devices, similar to biological neural systems, are able to realise both signal transmission and learning functions, where signal transmission is carried via the channel medium and synaptic weights are modulated

independently via the gate terminals.<sup>21,23,24</sup> The excitatory post synaptic conductance (EPSC) is measured as the time dependent channel conductance after the application of a voltage pulse on the gate electrode. If the EPSC signal lasts from a few seconds to tens of minutes, it is considered as the analogue of a Short Term Memory (STM) in psychology, whereas an EPSC signal lasting from a few hours to a lifetime is considered as a Long-Term Memory (LTM) transition.<sup>29</sup> Recent demonstration of synaptic properties using solution processed Organic core-sheath nanowire synaptic transistors revealed energy consumption for a single spike operation of 12.3 fJ.<sup>30</sup> However, short life time and poor reliability and mobility of organic materials and liquid electrolytes are a major concern for realising high performance electronic devices. Transparent conducting oxide (TCO) based synaptic devices hold great promise in realising energy efficient synaptic operation and spike timing dependent plasticity and short-term to long-term memory transitions have been demonstrated using Indium Zinc Oxide thin film transistors with nanogranular Silicon dioxide based proton conductor films as insulators.<sup>31-33</sup> The main drawback of such synaptic devices are the requirements of humidity to function as a synaptic FET, where the proton conductivity in the phosphorus-doped nanogranular SiO<sub>2</sub> films is facilitated by absorbed water molecules in the nanoporous film.<sup>33,34</sup> Short term synaptic plasticity is demonstrated with aqueous gated Indium Gallium Zinc oxide (IGZO) synaptic devices using water and salt as gate electrolyte.<sup>35</sup> However, dissolution of the IGZO films in water and irreversible electrochemical reactions at interface are a major concern in these types of devices.<sup>36</sup> TCO devices employing a ferroelectric gate insulator have also been reported to show EPSC behaviour.<sup>28,37</sup> The progressively higher programming voltage required to fully reverse the ferroelectric polarisation in these types of devices poses a significant challenge in realising synaptic devices with low operation voltage. The performance of the synaptic devices presented in this study are not

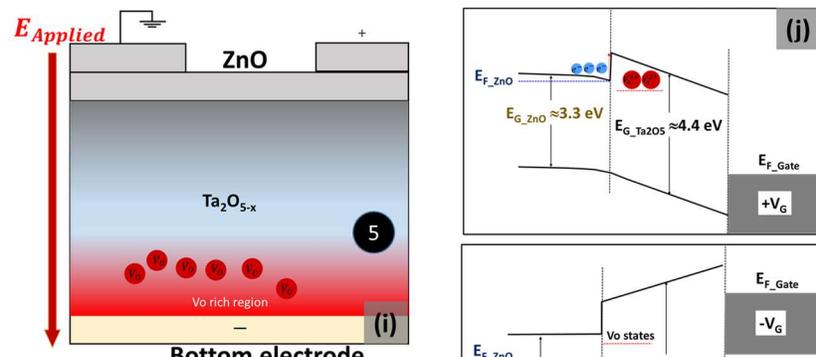
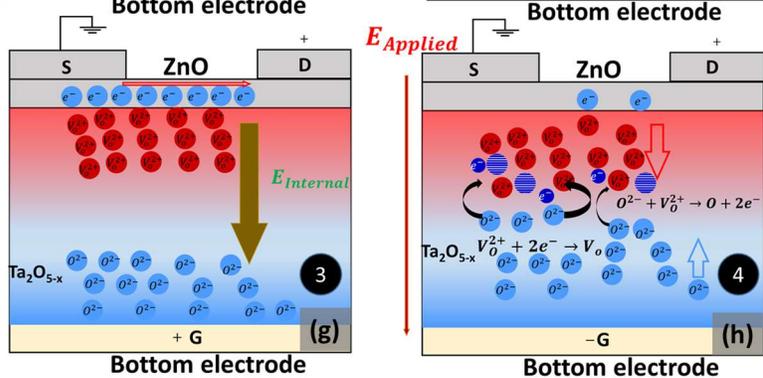
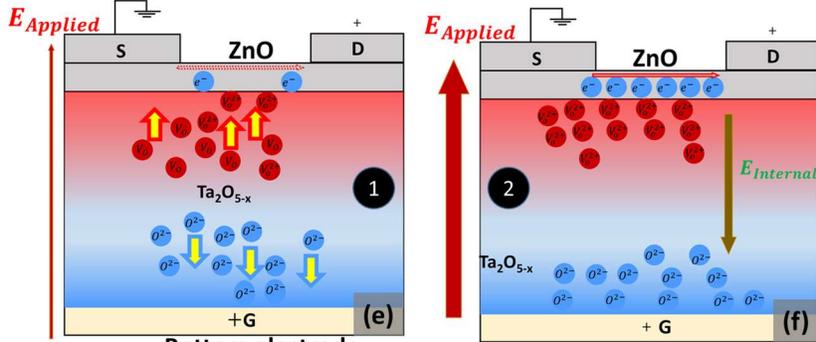
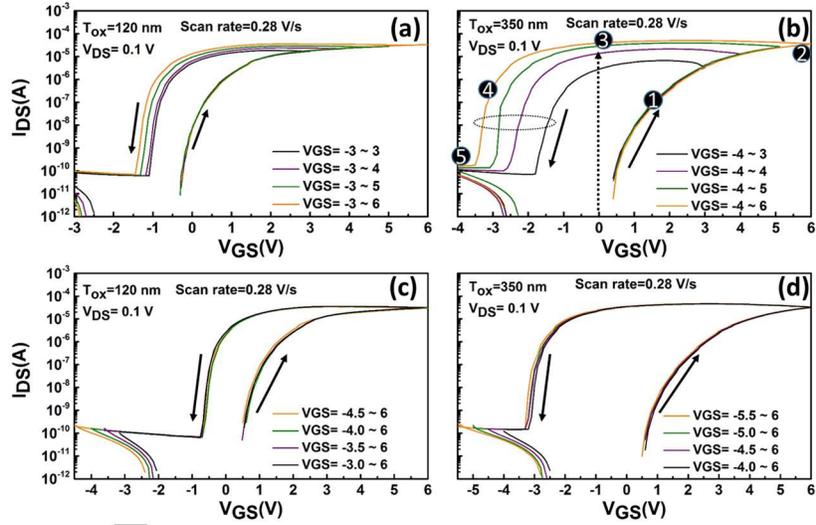
dependent on environmental factors and developing such synaptic transistors with biocompatible materials such as ZnO offers new possibilities for realising energy efficient compact synaptic memory devices that feature lower processing time and cost.

## 2. EXPERIMENTAL METHODS

Bottom gated TFTs were fabricated on glass using conducting Indium Tin Oxide (ITO, 20  $\Omega$ /square) as the gate, Tantalum Oxide ( $\text{Ta}_2\text{O}_5$ ) as gate insulator with different thicknesses (120, 200, 275 and 350 nm) and 40 nm Zinc oxide in all cases as channel via Radio Frequency sputtering from 2" solid ceramic targets (99.99%). Mild acid etching was used to define the ZnO mesa regions protected underneath the photo resist. The devices were subjected to thermal annealing at 80<sup>0</sup> C for 24 hrs. Patterning of the source/drain regions and deposition of Aluminium metal S/D contacts were achieved using standard photolithographic patterning, thermal evaporation and finally lift off in organic solvents. The capacitance characteristics were measured using an Agilent E4980A LCR meter. The electrical characteristics of the ZnO-TFTs were measured using a Keithley (4200 SCS) interfaced with a Desert Cryogenic probe station.

## 3. RESULTS AND DISCUSSION

The dependence of the width of the memory window with respect to the range of the positive gate voltage is shown in Figs 1a&b. The devices display a clear anti-clockwise hysteresis widely recognized in gate insulators with mobile ionic charges.<sup>38,39</sup> A high on-off ratio of  $10^7$ - $10^8$  and subthreshold swing  $\sim$ 100 mV/dec and a low gate leakage current  $<$  1nA are measured. A noticeable variation of the memory window with a positive gate bias range is observed in the case of 350 nm oxide as compared to a 120nm oxide device due to the higher amount of mobile charges



● ionised oxygen vacancy    ● Oxygen ions  
● oxygen atoms                      ● electrons

**Figure 1.** Dual sweep transfer characteristics of ZnO TFTs with different Tantalum oxide thicknesses a & c) 120 nm b) & d) 350 nm. In figs a & b, the lower limit of the  $V_{GS}$  sweep range is kept at a constant value (-3 or -4V) and the upper limit is gradually increased from 3 to 6V in consecutive dual sweep I-V measurements. In figs c & d, the lower limit of the  $V_{GS}$  sweep range is gradually increased from -4.5 to -3V (fig c) and -5.5 to -4V (fig d) while keeping the upper limit fixed at +6V. A hysteresis dependent upon the maximum applied  $V_{GS}$  is observed in a & b, while negligible effect is observed in figs c & d. e) A schematic of the junction structure corresponding to the forward sweep when  $V_{GS} \sim 1-2V$  (scenario 1), the applied electric field drives the doubly ionised oxygen vacancies and oxygen ions in opposite directions. Fig f) shows the separation of the vacancy/ionic components at  $V_{GS}=6V$  (forward sweep) resulting in an internal field opposite to the dominant external applied (red arrow). The positive oxygen vacancies at the channel-oxide interface result in a higher electron concentration in the ZnO channel (scenario 2). Fig. g) reveals the structure corresponding to the reverse sweep with  $V_{GS} \sim 0V$ . As the gate voltage reduces from 6V to smaller positive values, the internal electric field (shown by a thick arrow) in the gate insulator dominates and maintains a high electron concentration in the channel for conduction (scenario 3). However, a further reduction of the gate voltage results in a recombination of the oxygen ions and ionised vacancies (scenario 4) as shown in (h). At the lower limit of the reverse scan (-3V), an oxygen vacancy rich region is restored near the bottom gate (i) represented by scenario 5. Fig. j) represents the band alignment corresponding to fig f ( $V_{GS} \sim +6V$ ). The diagram shows a band offset of  $\sim 1.1$  eV for electrons at the ZnO/Ta<sub>2</sub>O<sub>5</sub> interface and ionised oxygen vacancy states in the Ta<sub>2</sub>O<sub>5</sub> band gap k) Schematic band diagram corresponding to fig (i) when the Fermi level in ZnO is pushed deeper into the band gap (off state condition).

in the former. A memory window as wide as 4V is realised within a sweep range of -4 to + 6V. A negligible dependence of the memory window in the negative gate bias range is observed when varied from -4.5V to -3V in the case of the 120nm oxide (fig 1c) and -5.5V to -4V for the 350nm oxide (fig 1d). The anomalous sweep range dependent memory window observed here can be understood based on the electric field induced ionic separation in the gate oxide. Here five different scenarios are considered.

Scenario 1: Fig 1e shows the schematic junction structure corresponding to initial charge separation in the dielectric medium by the applied positive gate bias ( $V_{GS} \sim 1-2$  V). The positive gate bias on the bottom gate electrode attracts the oxygen ions (negative) towards the gate/gate insulator interface and repels the ionised oxygen vacancies (positive) towards the channel/gate insulator interface resulting in an oxygen vacancy rich or poor region towards the channel interface or gate interface respectively.<sup>40</sup>

Scenario 2: The magnitude of the internal field increases with increase in upper limit of the  $V_{GS}$  sweep. The accumulated positive charge at the channel/insulator interface results in a similar image charge with opposite polarity (electrons) in the channel layer that drift in the direction from source to drain by the applied drain field (fig 1f).

Scenario 3: As the gate voltage is reduced from its upper limit (6V), the internal field becomes gradually dominant and maintains the electron concentration in the ZnO channel even at  $V_{GS} \sim 0$ V (fig 1g). This results in the counter-clock wise hysteresis as revealed in the I-V characteristics (fig 1a-d). It is worthwhile to note that reverse sweep conductance level increases with an increase in the  $+V_{GS}$  limit (fig 1b,  $+V_{GS}$  limit varying from 3 to 6V).

Scenario 4: As the gate voltage is reduced to a further negative value in the reverse direction, it results in a recombination of ionised oxygen vacancies and negatively charged oxygen ions causing the internal field to vanish (fig 1h).

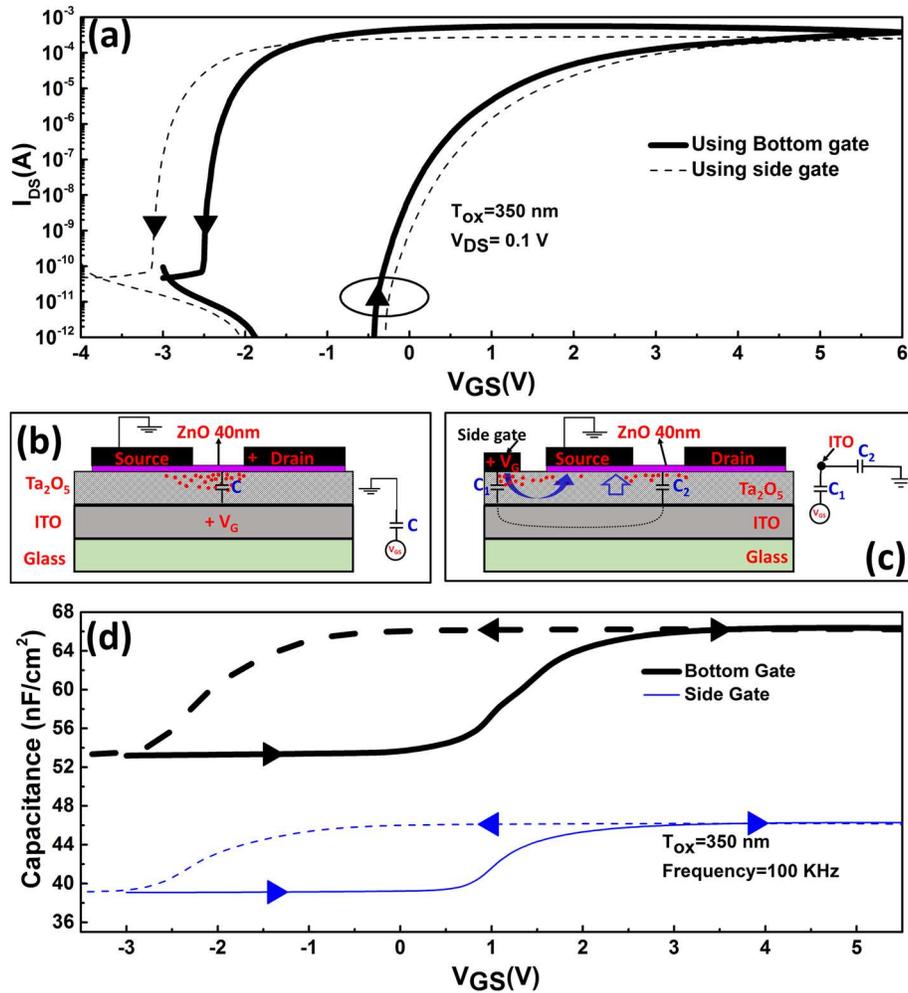
Scenario 5: When the reverse gate voltage scan attains a higher negative value, an oxygen vacancy rich region is formed near the gate electrode interface (fig 1i). It is revealed here that the anomalous counter-clockwise hysteresis arises from the positive gate sweep and application of a negative gate bias restores the charge separation to its initial state. This is evident from the negligible dependence of the lower limit of the gate sweep range on the observed hysteresis.

Fig 1j shows the schematic band diagram of the ZnO/Ta<sub>2</sub>O<sub>5</sub> interface where a finite band offset of ~ 1.1 eV for electrons in ZnO prevents the direct leakage of electrons into the Ta<sub>2</sub>O<sub>5</sub> layer. The ionised oxygen vacancy states are also highlighted in the band gap of Ta<sub>2</sub>O<sub>5</sub> using the previously reported activation energy for oxygen vacancy diffusion in Ta<sub>2</sub>O<sub>5</sub> of 1-1.3 eV.<sup>41</sup> Fig 1k shows the schematic band alignment corresponding to  $V_{GS} \sim -3V$ , where the ZnO fermi level is deep in the band gap resulting in no significant conduction in the channel (off state). A comparison of the performance of the memory of the TFTs from this study with other reported ZnO based TFTs is shown in Table 1. The dielectric constants of the gate insulators in these devices are also surmised. In the case of ferroelectric TFTs demonstrated using Poly(vinylidene fluoride-trifluoroethylene), P(VDF-TrFE) and other ferroelectric gate insulators<sup>42, 44,47</sup>, a sufficiently high programming voltage was required to fully reverse the ferroelectric polarisation. It is evident that the memory FETs demonstrated here can efficiently program the on and off state conditions within a lower voltage range of  $\pm 4V$  in comparison to other FETs. This is attributable to the enhanced interface capacitance between the gate dielectric and channel realised by the mobile ions in the Ta<sub>2</sub>O<sub>5</sub> solid electrolyte, resulting in an efficient coupling between the channel and gate electrodes.

Semiconductor/Insulator	Dielectric const. of Insulator	W/L ( $\mu\text{m}/\mu\text{m}$ )	$V_G$ range (V)	Memory Window (V)	Memory on-off ratio	Reference
ZnO/P (VDF-TrFE)*	11	495/90	$\pm 20$	15	$10^3$	42,44
#IGZO/ chicken albumen	5.3-6.1	40/20	$\pm 20$	11.8	$10^6$	45,46
Nano wire ZnO/ BaTiO <sub>3</sub> &	500-6900	0.1/3	$\pm 15$	$\sim 7$	$10^4$	43,47
Nano wire ZnO/ Pb (Zr <sub>0.3</sub> Ti <sub>0.7</sub> )O <sub>3</sub> (PZT) <sup>‡</sup>	250-350	3/0.08	$\pm 5$	7	$10^3$ - $10^4$	48,49
Nano wire ZnO/ SiO <sub>2</sub> <sup>§</sup>	3.9	3/.05	$\pm 25$	20	$10^3$	50
ZnO/ PVP- P(VDF/TrFE)	11	540/90	$\pm 70$	51	$\sim 10^2$	51
Al-Zn-Sn-O/ P(VDF- TrFE)	11	20/10	$\pm 6$	1.8	$\sim 10^3$	37
ZnO/Ta <sub>2</sub> O <sub>5</sub>	21	300/10	-4 to + 6	4	$10^5$ - $10^6$	This work

Table 1: Summary of the memory performance of Zinc Oxide based thin film transistors. \* poly vinylidene fluoride trifluoroethylene, # Indium Gallium Zinc Oxide, & Barium Titanate, § Silicon Oxide. ‡ Lead zirconium titanate.

The transfer characteristics of a device employing a side or in-plane gate in comparison to that with a bottom gate are shown in Fig 2a, where the voltage applied on the in-plane-gate is coupled to the channel layer through the conducting Indium Tin Oxide and Ta<sub>2</sub>O<sub>5</sub> layers. The corresponding capacitance- gate voltage characteristics using bottom and side gates are shown in



**Figure 2.** a) Dual sweep I-V data of ZnO TFTs using a bottom gate (bold lines) and side gate (dotted lines) for a 350 nm gate oxide TFT. The forward and backward sweep directions are indicated by arrow heads on the curves b) Schematic device structure with equivalent channel-gate capacitor circuit in the case of a bottom gate (b) and side gate geometries (c). d) Comparison of the dual sweep CV characteristics of the same device acquired at a frequency of 100 KHz using bottom (thick black lines) and side gate (thin blue lines) geometries.

fig 2b. The separation between the in-plane gate and the channel region is  $240\ \mu\text{m}$  and the oxide thickness is 350nm. As shown in figs 2b & c, in the bottom gate geometry, the gate and channel are coupled through a single capacitor C, while in the side gate geometry (fig 2c), the equivalent

circuit shows two capacitances  $C_1$  and  $C_2$  between the side gate and channel. Hence a lower capacitance is expected in the side gate configuration. The junction structure shown in figs 2b & 2c also reveals the ionised oxygen vacancy motion under a positive voltage on the side or bottom gate. Capacitance-gate voltage characteristics shown in fig 2d reveal a capacitance ratio of  $\sim 1.44$  between values of the accumulation capacitance in the bottom and side gate geometries. This indicates that the coupling of the side gate to the channel region is not entirely through the bottom ITO conducting layer and that laterally coupled ZnO TFTs can be realised without a bottom conducting layer, as reported in ref<sup>32</sup>. From the C-V measurements, the dielectric constant ( $\kappa$ ) of Ta<sub>2</sub>O<sub>5</sub> is measured as  $\sim 21$  at an AC frequency of 1 MHz and for a known thickness of 350 nm. The dispersion in frequency of the insulator capacitance is compared for oxide thicknesses of 120 and 350 nm in a metal-insulator-metal geometry and reveals that dispersion is very identical to gate insulators with mobile charge in earlier reports on memory/synaptic devices<sup>32,33</sup>. (supporting info fig S1)

The analogy between a biological synapse and the transparent oxide based synaptic device is depicted in fig 3a & b. The equivalent role of memory behaviour in biological systems is played by the voltage spike driven synaptic behaviour enforced by ionised oxygen vacancies in the ZnO/Ta<sub>2</sub>O<sub>5</sub> device (fig 3b). Accumulation of the positively charged ionised oxygen vacancies at the channel interface results in modulation of the channel conductance as explained in fig 1f. To demonstrate the synaptic behaviour, a pre-synaptic spike (25ms, 200 mV) is applied on the gate of the TFT as an external stimulus and a corresponding excitatory post synaptic current (EPSC) from the source/drain output terminal is measured as the synaptic weight, using a drain voltage of 200 mV (fig 3c). The EPSC signal attains a peak value of  $\sim 7$  nA at the end of the spike and then decays back to a base level of  $\sim 3$  nA. The calculated energy dissipation of a single spike event is  $\sim 35$  pJ,

significantly lower than that reported for zinc oxide based synaptic devices ( $\sim 160$  pJ)<sup>33</sup> and comparable to the single spike energy consumption reported for a CMOS based artificial synaptic system.<sup>2</sup> (The power consumption in this CMOS based system is a function of spike rate, the average distance travelled by spikes, and the average number of active synapses per neuron. In a situation where the neurons fire on average at 20 Hz and have 128 active synapses, the energy consumption is 26 pJ per synaptic event). Two terminal based metal oxide resistive switching memory (RRAM) based synaptic devices have earlier been reported to have a single spike energy consumption of less than 1 pJ<sup>27</sup> and this value is significantly smaller than the present ZnO based devices. However, the energy consumption for a single spike in our device can be further reduced by scaling the device dimensions and adjusting the device threshold voltage. It is noteworthy that the operating voltage employed here to emulate synaptic properties (100-200 mV) is significantly smaller than in other technologies (1-10V) (see fig. 11 of the review article by Kuzum et. al., in<sup>53</sup>).

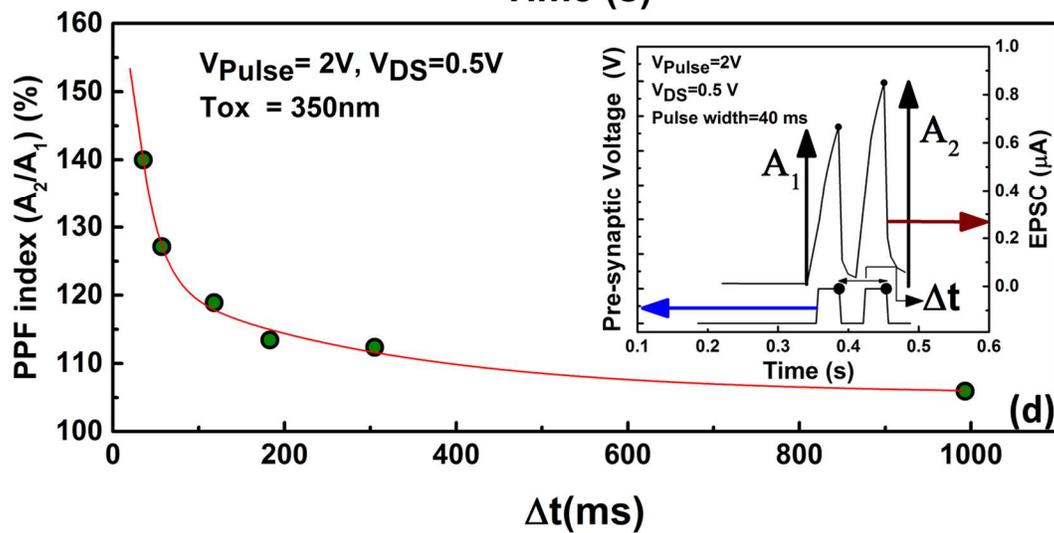
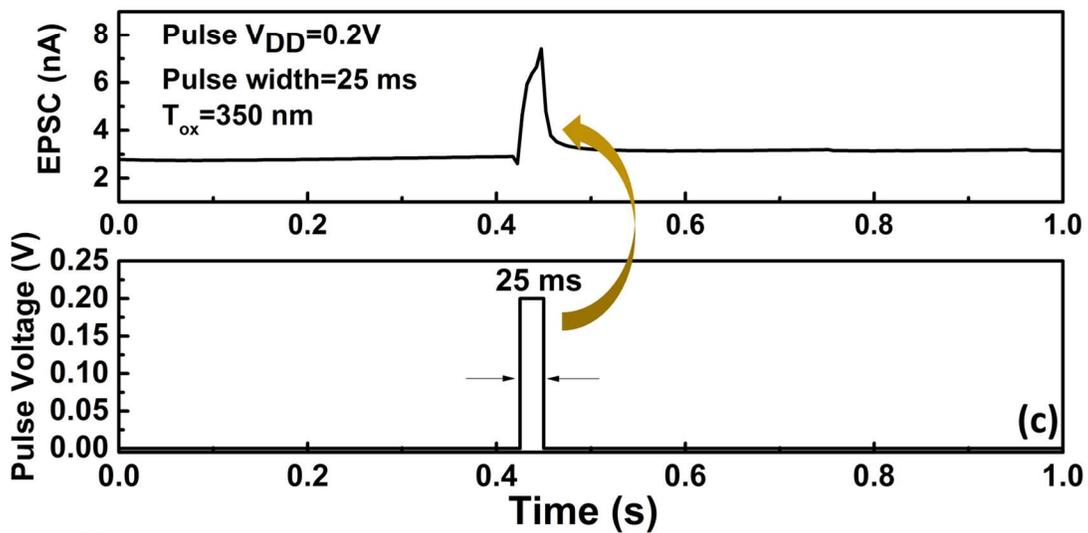
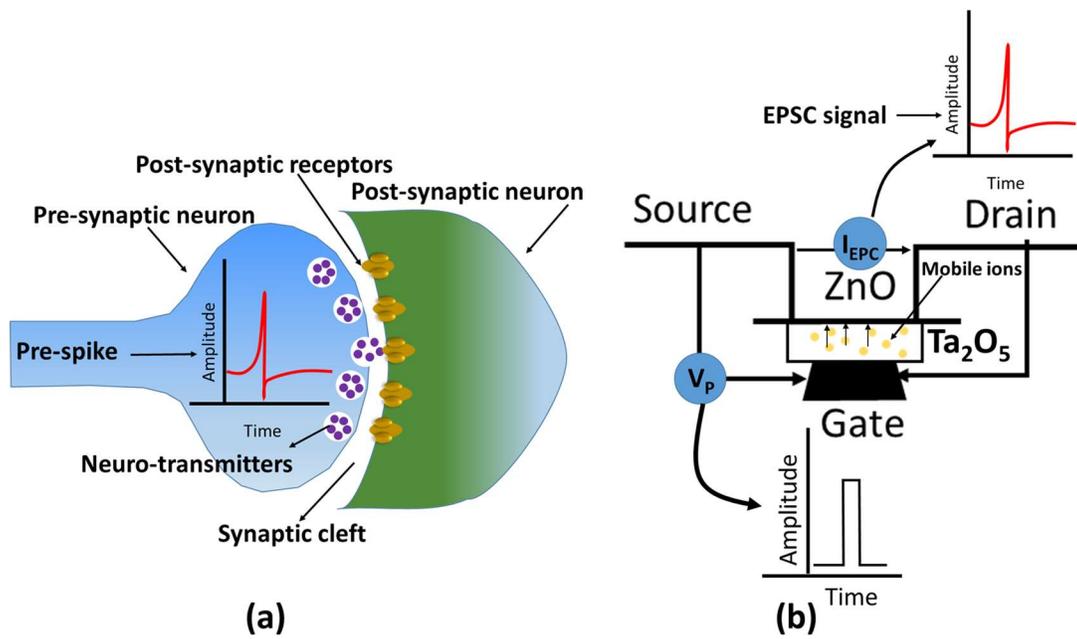


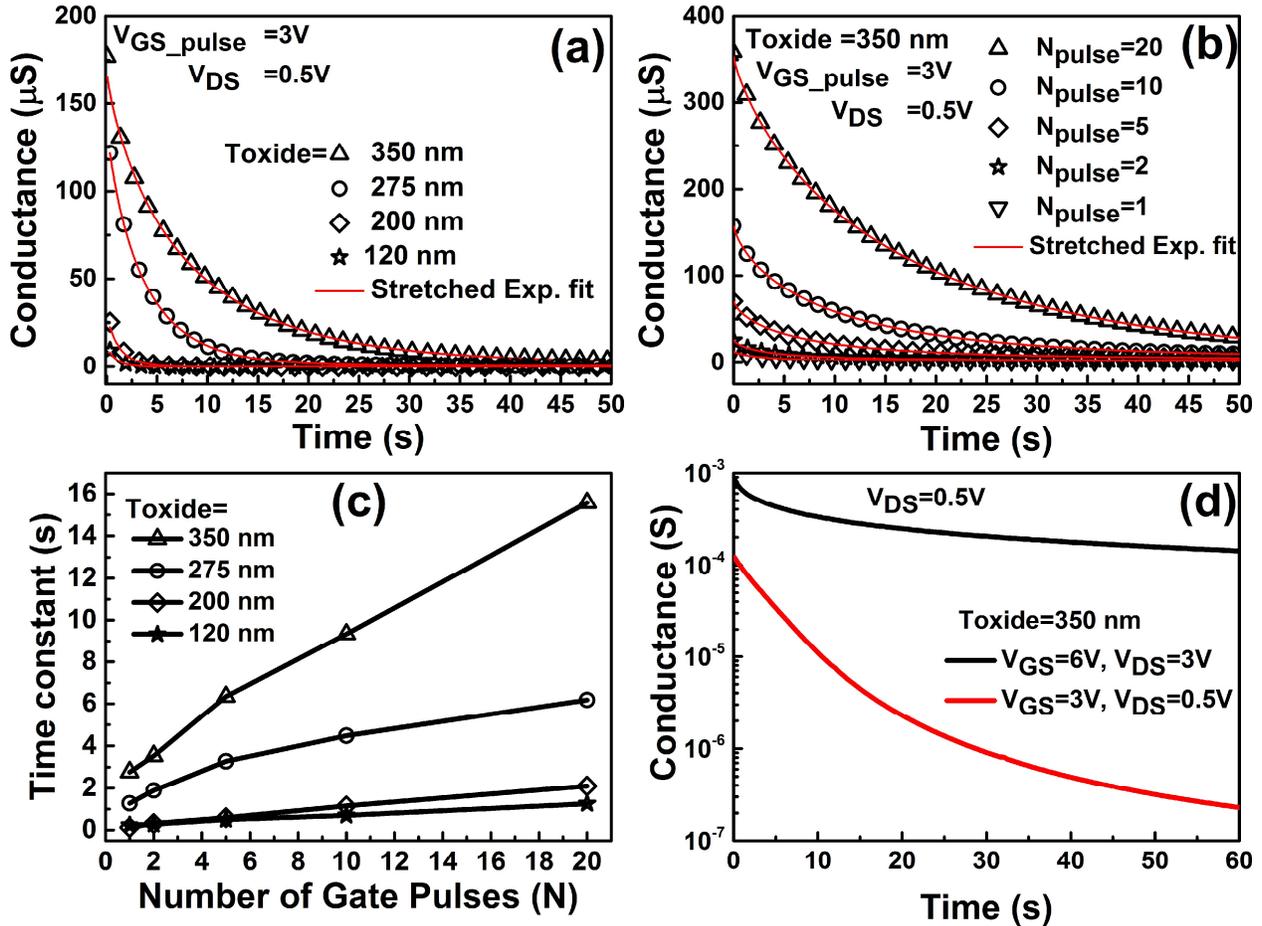
Figure 3: a) A schematic diagram highlighting the analogy between a neural synapse (a) and an artificial synaptic device reported here (b). Post synaptic strength in the former is decided by the amount of release of neuro transmitters, whereas in the latter, it is the movement of ions to and fro within the gate insulator c) Excitatory Post Synaptic Current (top panel) triggered by a presynaptic spike (200 mV, 25 ms) (bottom panel). The EPSC is measured with a  $V_{DS}$  of 200 mV d) Paired pulse facilitation property of the synaptic device is demonstrated using two presynaptic spikes at the gate terminal with inter-spike interval time ( $\Delta t$ ) varying from 40-1000 ms. Here  $A_1$  and  $A_2$  (figure inset of d) represent the amplitudes of the first and second EPSCs, respectively.

The property of the paired pulse facilitation (PPF) of the ZnO synaptic devices is shown in fig 3d. PPF is a form of short-term synaptic plasticity and the PPF index is measured as the ratio of the postsynaptic response to the second presynaptic spike over the response to the first spike. A maximum PPF index of 140 is measured with an inter-spike interval of 40 ms. At longer spike intervals, the accumulated charge at the semiconductor/ gate insulator drifts gradually to the gate insulator whereas if a small inter-spike interval is used, the mobile charges triggered by the first pulse that reside near the channel/insulator interface, augmented with the second pulse, results in a stronger EPSC response as shown in fig 3d.

The synaptic response of devices with four different Ta<sub>2</sub>O<sub>5</sub> gate insulator thicknesses of 120, 220, 275 and 350 nm are analysed in fig 4a which shows the decay of the post synaptic conductance ( $I_{DS}/V_{DS}$ ) after the application of 10 pre-synaptic spikes (3V, 300 ms) for various gate insulator thicknesses. The decay data can be well fitted using a stretched exponential function described earlier by Kohlrausch <sup>54</sup>

$$G = (G_0 - G_\infty) \exp \left[ - \left( \frac{t}{\tau} \right)^\beta \right] + G_\infty \quad (1)$$

where  $t$  is the time after the end of the pre- synaptic spike,  $\tau$  is the retention time,  $G_0$  is the channel conductance at  $t = 0$ ,  $G_\infty$  is the resting current and  $\beta$  is the stretch index, typically between 0 and 1.



**Figure 4.** a) ZnO channel conductance decay after 10 gate pulses of 3V (300 ms) for different oxide thicknesses. b) channel conductance decay after applying different number of gate pulses for 350nm oxide TFT c) Time constant extracted using the stretched exponential fit (Equation 1) d) Comparison of the channel conductance decay measured at  $V_{DS}=0.5V$  after the application of a 3V gate pulse (red line) and a simultaneous gate (6V) and drain pulse (3V) for 3s showing a permanent retention behaviour (black line) for a 350 nm oxide.

The decay of the EPSC signal with pulse numbers varying from 1 to 20 is shown in fig 4b. The retention time constants extracted for various pulse numbers corresponding to the four different oxide thicknesses are shown in fig 4c. The retention time increases with pulse number and gate insulator thickness. An obvious 8-fold increase in retention time is observed for an insulator thickness of 350 nm, when the pulse number changes from 1 to 20. This shows that the memory level could be strengthened through a process of rehearsal similar to that in biological systems. Based on the “multi-store model” in psychology proposed by Atkinson and Shiffrin<sup>50</sup>, a biological memory can be divided into the following three categories, a) sensor memory b) short term memory (STM) and c) long term memory (LTM). The sensory memory is concerned with a perception of touch, smell or a visual pattern that lasts only for a fraction of a second in memory and the sensation is further stored in a short term memory (STM) which lasts for a few seconds. Important information is gradually transferred to a long term memory which can often be memorised in the life time of an individual through the process of rehearsal. In figure 4d, it is shown that these ZnO TFTs are capable of storing information for a short time by controlling the memorisation pulse amplitude applied at the gate. A short term memory retention property is demonstrated by the application of a  $V_{GS}$ -pulse = 3V, 300 ms. The LTM feature is shown by applying a sufficiently high gate (6V) and drain pulse (3V) simultaneously for a period of 3s. The long term retention behaviour is found to be stable up to several hours (see supp info Fig S1). Moreover, the synaptic behaviour exhibited by these devices is independent of environmental factors and strong synaptic properties are prevalent when tested after storing the devices in a vacuum of  $10^{-3}$  mbar for an arbitrary period of 16 hrs which reveals that environmental humidity has little impact on the synaptic properties. (see supporting info Fig S2). The relaxation of the segregated ionised vacancies to their equilibrium positions away from the channel interface results

in the short- term memory retention and the long term memory behaviour may be attributed to the electrostatic doping of the channel layer by the ionised oxygen vacancies similar to the electrostatic doping of IZO layer by mobile protons in nanogranular SiO<sub>2</sub>/IZO TFTs reported elsewhere.<sup>33</sup>

The EPSC response of the device when 10 pre-synaptic pulses of width 40 ms and amplitude 2V are applied on the gate is shown in fig 5a. A large synaptic response (~2 μA) even for a narrow spike width of 40 ms is observed. In fig 5b), The EPSC response of the device against a stimulus train of different pulse widths is shown. The stimulus train at each frequency consists of 10 pre-synaptic spikes of 2 V applied to the gate terminal at a V<sub>DS</sub>= 0.5 V, applied between the source and drain electrodes. It is obvious that a longer pulse width results in stronger EPSC values and longer retention time for the memorization event. Fig 5c represents the EPSC response to a stimulus train with a constant pulse width of 25 ms but having different pulse frequencies ranging from 1 to 33 Hz. The stimulus train consists of 10 spikes at each frequency and a pulse amplitude of each spike

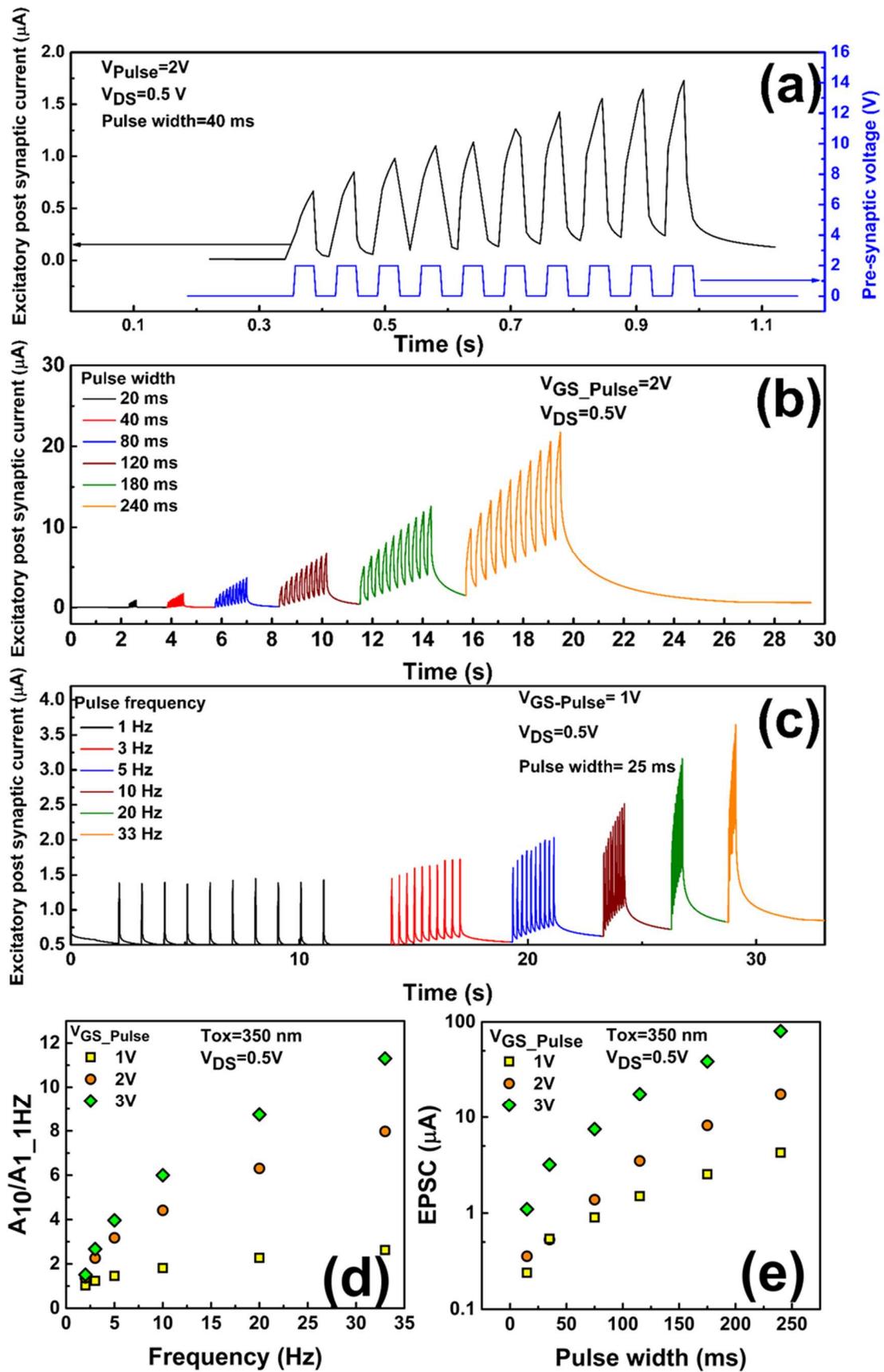


Figure 5: a) Excitatory post synaptic current (EPSC) measured from a ZnO TFT (W/L=300/10  $\mu\text{m}$ ) using 10 pre-synaptic pulses of width 40 mS, the gate pulse used for the stimulation of channel conductance is shown in the bottom half of the figure (in blue) b) EPSC signal with varying pre-synaptic pulse widths from 20ms to 240 ms (duty cycle = 50%), 10 gate pulses ( $V_{\text{pulse}}= 2\text{V}$ ) were used in each case c) EPSC signal with a constant pulse period of 25 mS where frequency is varied from 1-33 Hz ( $V_{\text{pulse}}=1\text{V}$ ) d) Pre-spike frequency Vs Excitatory post synaptic current (EPSC) gain ( $A_{10}/A_1$ ) for various pre-synaptic voltages (1-3V) where  $A_{10}$  represents the amplitudes of the 10<sup>th</sup> EPSC signal and  $A_1$  is the amplitude of the first post synaptic signal in the spike train (frequency=1 Hz) e) pre-spike pulse width Vs EPSC magnitude measured for various spike voltages (1-3V)

is 1V. The EPSC response is captured using a drain bias of 500 mV. When the frequency is small (1Hz) the EPSC gain is nearly unity and strongly enhanced when the frequency of the stimulus spikes and pre-synaptic voltage rises to 33 Hz and 3V respectively(fig 5d). This reveals an ability of the ZnO synaptic devices to function as a dynamic high-pass filter for information transmission that can be exploited in realizing synaptic activities involving transmission of firing patterns with low initial probability of neurotransmitter release such as parallel fibre synapses.<sup>55</sup> The EPSC shows a strong dependence on the pre-spike pulse width and shows a saturation value above 250 ms pulse width (fig 5e).

Finally, in fig 6, the endurance of the device is examined by repeatedly applying potentiating (+ 0.5 V, 10 ms) and depressing (-0.5V,10 ms) (P/D) pulses at the gate terminal. The EPSC values are recorded using a drain voltage of 500 mV for a fresh device (fig 6a), after  $2.8 \times 10^6$  (fig 6b) and  $7.1 \times 10^6$  P/D cycles (fig 6c). The devices retained 85% of their initial EPSC value after  $7.1 \times 10^6$  P/D cycles of continuous operation revealing stability in their operation.

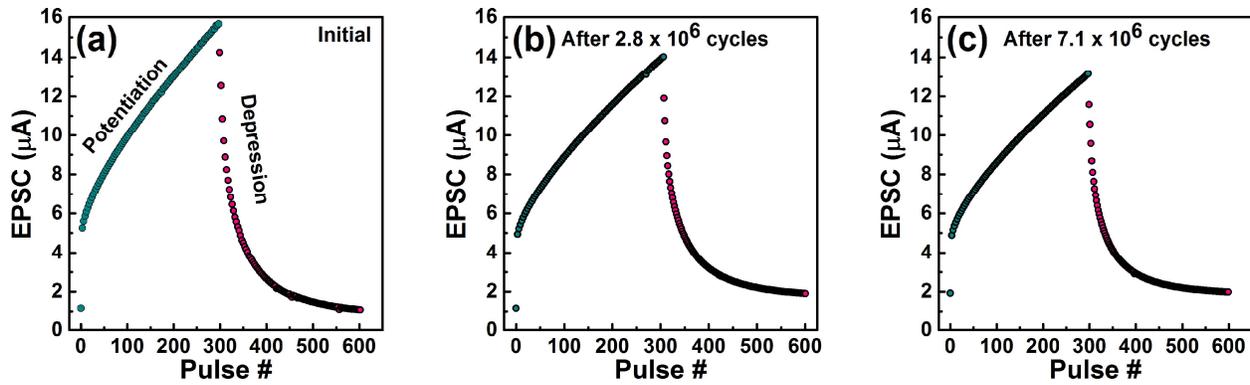


Fig 6: Synaptic response of the ZnO TFTs after repeated potentiation (0.5V, 10 ms) and depression pulses (-0.5V, 10 ms) applied at the gate terminal. EPSC response is measured using a drain voltage of 500 mV for a) fresh device, after  $2.8 \times 10^6$  (b) and  $7.1 \times 10^6$  (c) P/D cycles. The pulse parameters for P/D measurements are 0.5V, 50 ms and -0.5V, 50ms respectively.

It is revealed here that single device level synaptic transmission and memory storage can be realized using ZnO TFTs with Ta<sub>2</sub>O<sub>5</sub> gate insulator. An artificial synaptic network with multiple pre-synaptic terminals to spatiotemporally modulate the post synaptic weight can be engineered using the proposed device structure. Moreover, the strong lateral coupling of the gate and channel demonstrated here dramatically simplifies the architecture of the synaptic network and synaptic properties can be further optimized by regulating the distance between the in-plane gate and the channel. These three terminal based synaptic devices shown here are able to realise signal transmission and self-learning processes simultaneously and offer a promising option for efficient neuromorphic systems.

#### 4. CONCLUSION

In summary, memory and synaptic behavior of low temperature processed ZnO/Ta<sub>2</sub>O<sub>5</sub> thin film transistors using a simple bottom gate geometry are demonstrated for the first time. A memory

window greater than 2V can be envisaged within an operational voltage of -3 to +4 V. The size of the memory window can be efficiency tuned by adjusting the gate insulator thickness. Short term and long term memory retention are demonstrated by regulating the magnitude of the pulse applied on the gate terminal. Plasticity and high frequency filtering synaptic functions are successfully mimicked. A strong lateral coupling of gate and the channel achieved through mobile ions in the gate insulator, very similar to neuro-transmitters, demonstrated here reveals the possibility to design three terminal synaptic FETs with in plane gate geometry. Further optimizing the device structure and dimensions, the single spike energy consumption can be lowered to realise a synaptic array with multiple pre-synaptic terminals to spatiotemporal modulation of the post synaptic weight.

- SUPPORTING INFORMATION

Additional characterization data including frequency dispersion of capacitance revealing mobile charges in the oxide, long term memory retention behavior of the ZnO device and synaptic response measured in vacuum and ambient environments to demonstrate the environmental stability of the devices.

- ACKNOWLEDGEMENT

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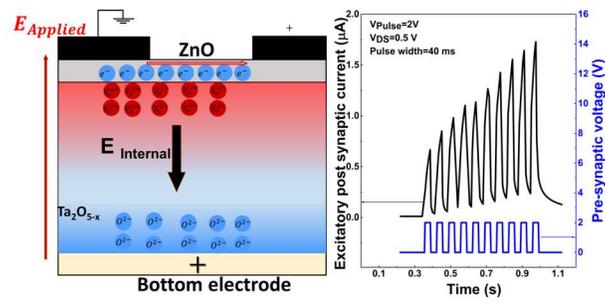
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# Table Of Content (TOC) Graphic



## Supporting information

A nanoionics based three terminal synaptic device using Zinc Oxide

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1) Comparison of the Oxide capacitance and role of mobile charges

The frequency dispersion of insulator capacitance is compared for oxide thicknesses of 120 and 350 nm in metal-insulator-metal geometry. This dispersion behaviour is identical to the gate insulators with mobile charge as revealed in earlier reports on memory/synaptic devices<sup>1,2</sup>

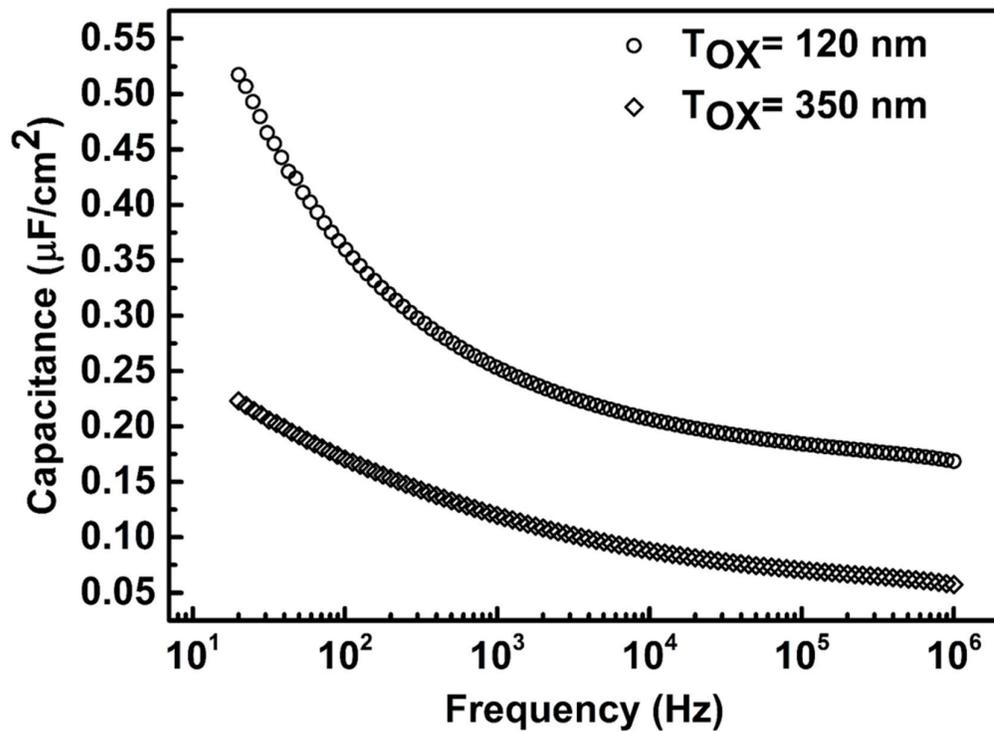


Fig S1: Dispersion of oxide capacitance with frequency for 120 nm and 350nm thick  $Ta_2O_5$  films measured in the frequency range 20 Hz - 1 MHz in a Metal/Insulator/Metal geometry.

## 2) Demonstration of long term memory retention in ZnO synaptic transistors

Long term memory retention properties of the device with dimension  $W/L = 300/10 \mu\text{m}$  is measured using the pulsing scheme shown in the inset of fig S2. A gate voltage pulse of magnitude 6V and drain voltage of 3V are simultaneously applied for a duration of 5s. The S/D conductance are monitored for a duration of 10,000s at  $V_{GS}=0\text{V}$  and  $V_{DS}=0.5\text{V}$ .

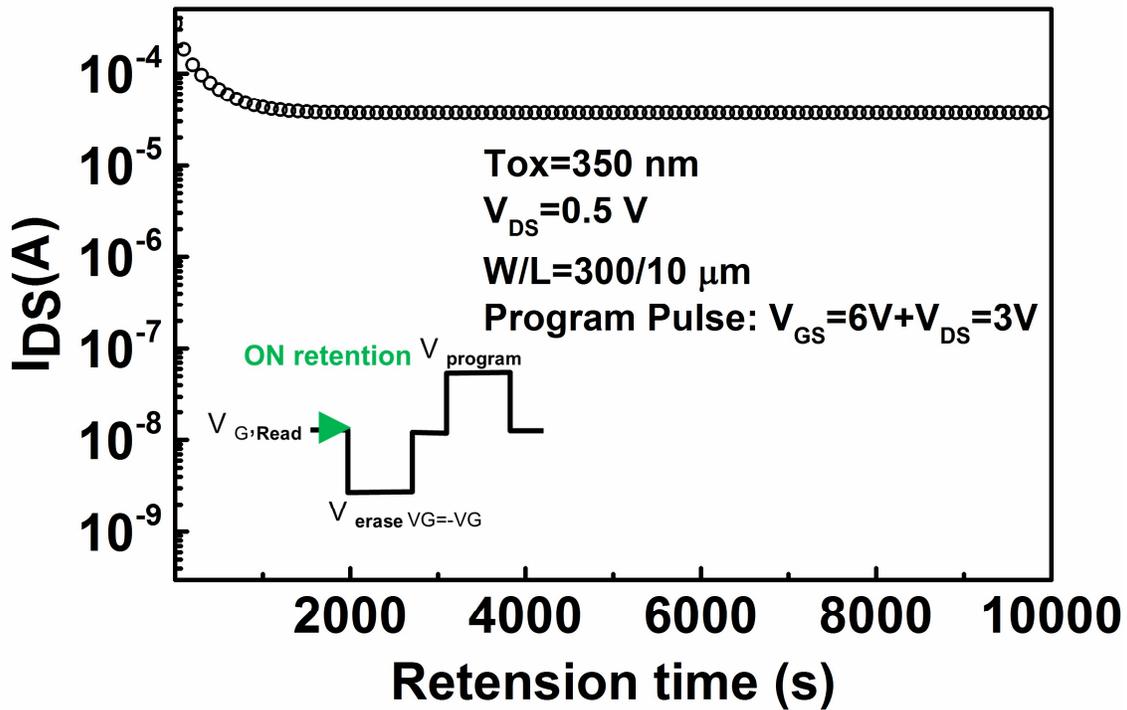


Fig S2: Decay of channel conductance measured at  $V_{DS}=0.5\text{V}$  and  $V_{GS, Read} = 0\text{V}$  after the application of a simultaneous gate (6V) and drain pulse (3V) for 5s shows a permanent retention behavior for a 350 nm oxide. The retention data is measured using the single pulse scheme shown in the inset of the figure.

### 3) Synaptic properties under vacuum and ambient conditions

In fig S3, it is shown that robust synaptic behavior can be observed under vacuum conditions ( $10^{-3}$  mBar). The figure reveals the comparison of synaptic behavior measured using a gate pulse of magnitude 3V, with a pulse duration of 240 ms. The slight difference in the channel conductance observed under vacuum and ambient conditions may be attributed to the shift in threshold of the devices under vacuum.

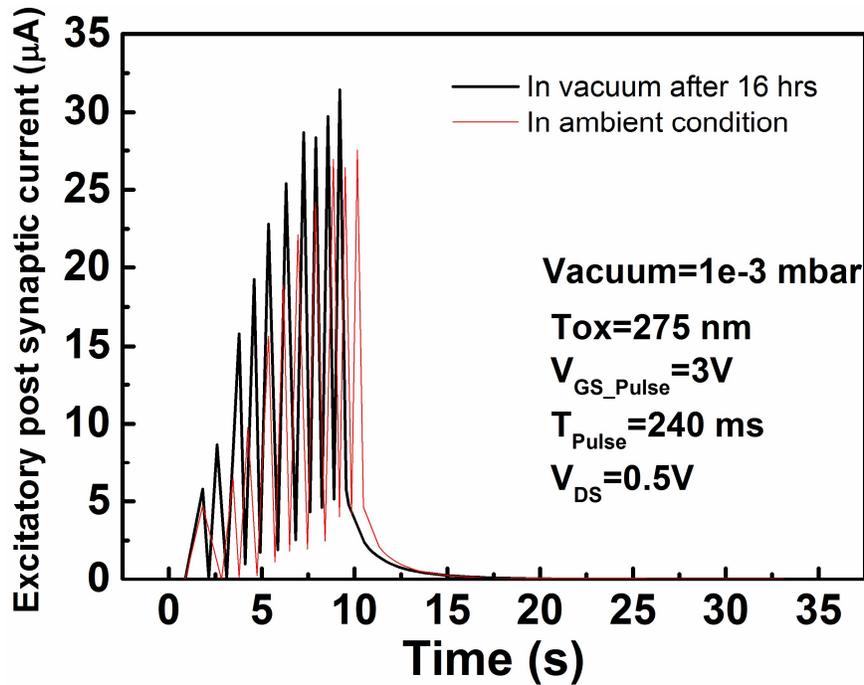


Fig S3: Synaptic properties of the ZnO TFTs measured under ambient conditions (red lines) and under vacuum of  $10^{-3}$  mbar (black lines) (after keeping the device for 16 hrs). The synaptic strength after 10 consecutive spikes reaches a peak value of 32  $\mu$ A, marginally higher than the value measured under ambient condition (27  $\mu$ A) presumably due to a small shift in threshold of the devices in vacuum. (The comparison reveals that synaptic properties of the ZnO/Ta<sub>2</sub>O<sub>5</sub> TFTs are not significantly affected by the humidity/environmental parameters.

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